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Voltage Scalling Based Traffic Light Controller Design on Virtex-7 FPGA Family

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Abstract

This is an apporach to design of energy efficient traffic light controller on Virtex-7 FPGA that consume low amount of power. There is a reduction of 46.31%, 70.11% and 82.58% in leakage power as the voltage is scale down from 1.8V to 1.6V, 1.4V and 1.2V respectively at ambient temperature 25^{o}C.There is a reduction of 52.48%, 75.59% and 86.96% in leakage power as the voltage is scale down from 1.8V to 1.6V, 1.4V and 1.2V respectively at ambient temperature 50^{o}C. There is a reduction of 46.31%, 70.11% and 82.58% in clock power as the voltage is scale down from 1.8V to 1.6V, 1.4V and 1.2V respectively at any value of ambient temperature.

Keyword: Verilog, FPGA, Energy Efficient design, Traffic Light Controller.

1.INRODUCTION:

In this work, Verilog is used as hardware description language for implementation of traffic light controller. It shows Red, Green and Yellow color at a predefined interval. Voltage scaling is used as energy efficient design. Traffic light controllers are used to control the movement of the vehicles. Power dissipation is measured on XPOWER simulator. In this paper we have to use Virtex-7 FPGA family to making energy efficient design traffic light controller. Y denotes Yellow, R denotes Red and G denote Green color of traffic light controller. There are two inputs and 12 outputs in design under consideration. We have generated RTL schematic, technology schematic. Top level schematic of Traffic Light Controller as shown in figure 1. It shows basic input required for traffic light controller and basic output required for our design under test. Verilog is a language which is similar to the C programming language, which was already widely used in engineering software development. A Verilog design consists of a hierarchy of modules. Synthesis software algorithmically transforms the Verilog source into a netlist, a logically equivalent description consisting only of elementary logic primitives (AND, OR, NOT, ip- ops, etc.) that are available in a speci c FPGA or VLSI technology. Virtex-7 is 28nm technology based FPGA. LVCMOS18 is the default IO standards.

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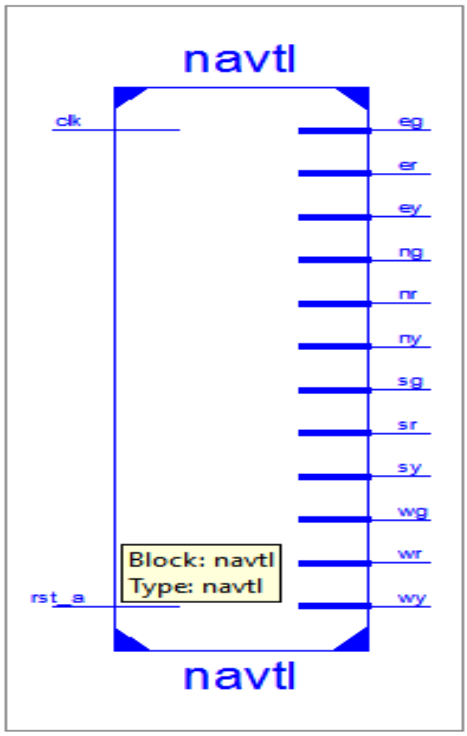

Figure 1 Top Level Schematic view of Traffic Light Controller.

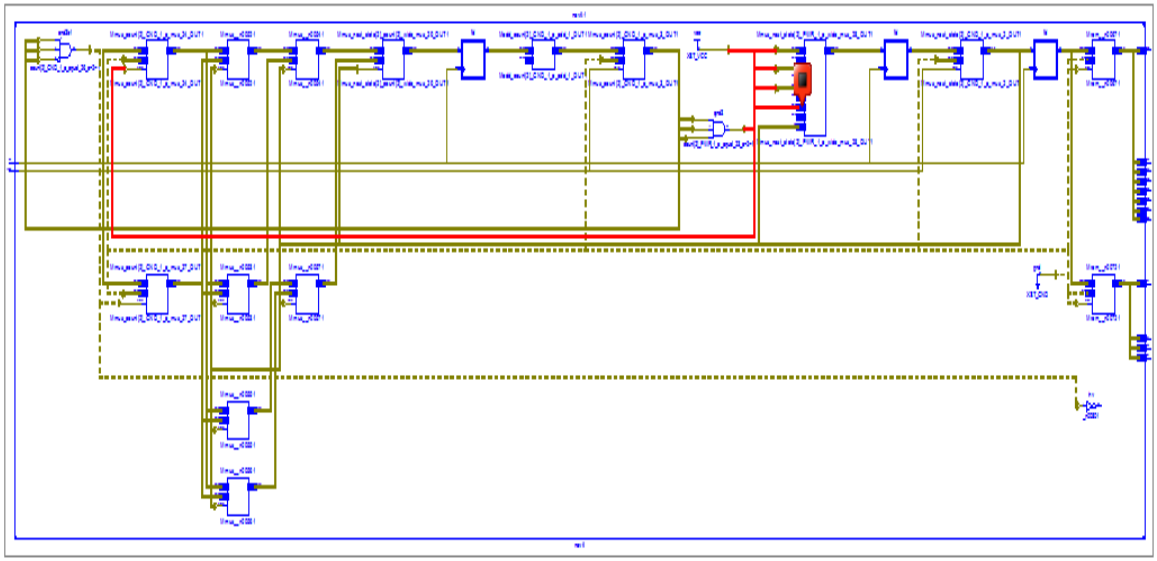

Figure 2 RTL Schematic view of Traffic Light Controller

Internal Architecture of RTL Schematic of traffic light controller is shown in Fig. 2. This architecture shows different multiplexer, gates and other basic primitive circuits used in RTL schematic. Technology schematic of our design is shown in Fig. 3.In this design we are using Number of Slice Registers, Number of Slice LUTs, Number used as logic, Number of occupied Slices, Number of slice register sites lost to control set restrictions and Number of bonded IOBs are 9,15,15,9,7 and 14 respectively.

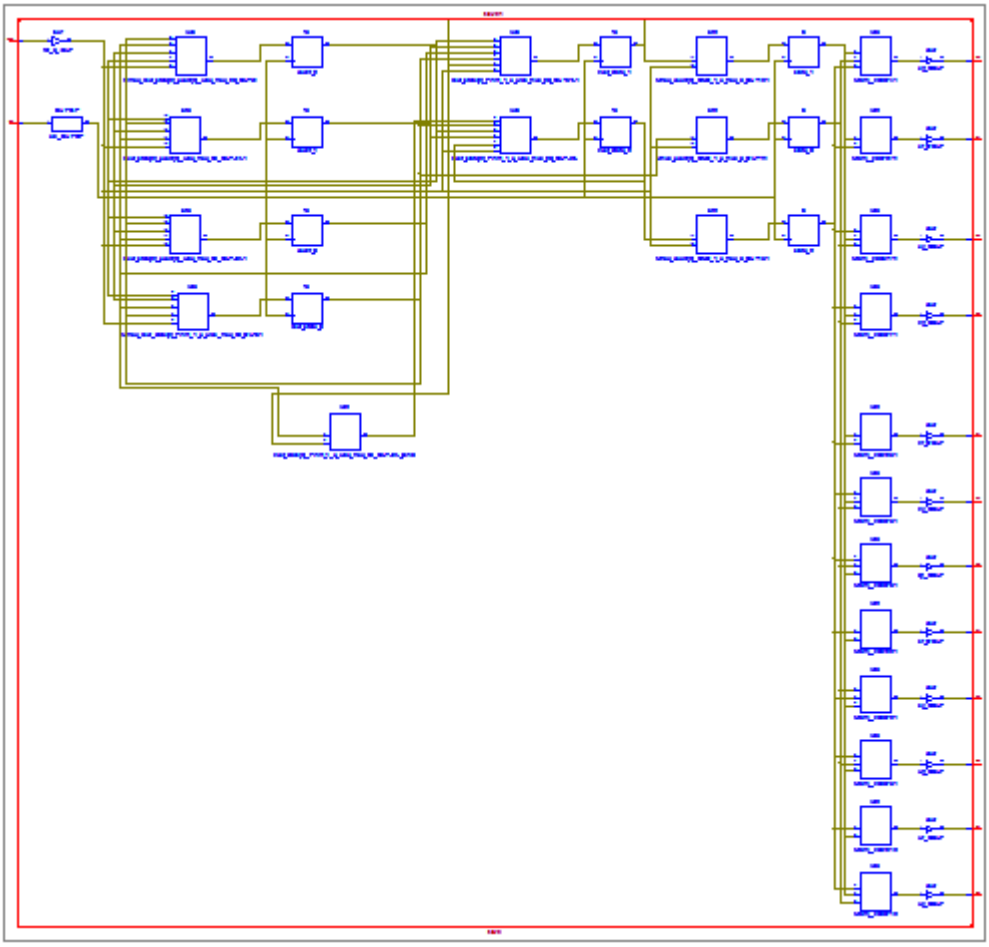

Figure 3 Internal Architecture of Technology Schematic view of Traffic Light Controller.

In the figure 3, Technology Schematic view of Traffic Light Controller are shown. This architecture shows different multiplexer, gates and other basic primitive circuits used in technology schematic.

2. RELATED WORK

Some researcher has work done on Simulation of voltage scaling aware mobile battery charge controller sensor on FPGA[1]. Some other researcher has work on Adaptive voltage scaling with in-situ detectors in commercial FPGAs[2]. Some other scientist has work on Energy Efficient Counter Design Using Voltage Scaling On FPGA[3]. Another researcher has worked on Leakage power reduction with various IO standards and dynamic voltage scaling in vedic multiplier on Virtex-6 FPGA[4]. Most of the researcher has worked on Design and implementation of a real-time traffic light control system based on FPGA[5]. Some author has Design of smart traffic light controller using embedded system[6]. Some of the other researcher has designed A 90nm low-power FPGA for battery-powered applications[7]. Some researcher has designed Low-power FPGA using pre-defined dual-Vdd/dual-Vt fabrics[8]. Another researcher has worked on Leakage power reduction with various IO standards and dynamic voltage scaling in vedic multiplier on Virtex-6 FPGA[9]. In our work we are using voltage scaling based design of energy efficient Traffic Light Controller on Virtex-7 FPGA family that consume low amount of power.

3. RESULT AND DISCUSSION

Table 1 Power dissipation on different value of supply voltage Vccint at 25°C.

Voltage	Leakage power
1.2	0.229
1.4	0.393
1.6	0.706
1.8	1.315

There is a reduction of 46.31%, 70.11% and 82.58% in leakage power as the voltage is scale down from 1.8V to 1.6V, 1.4V and 1.2V respectively as shown in figure 4 and table 1.In which we have used output load capacitance value is 5pF and clock pulse period is 5ns.

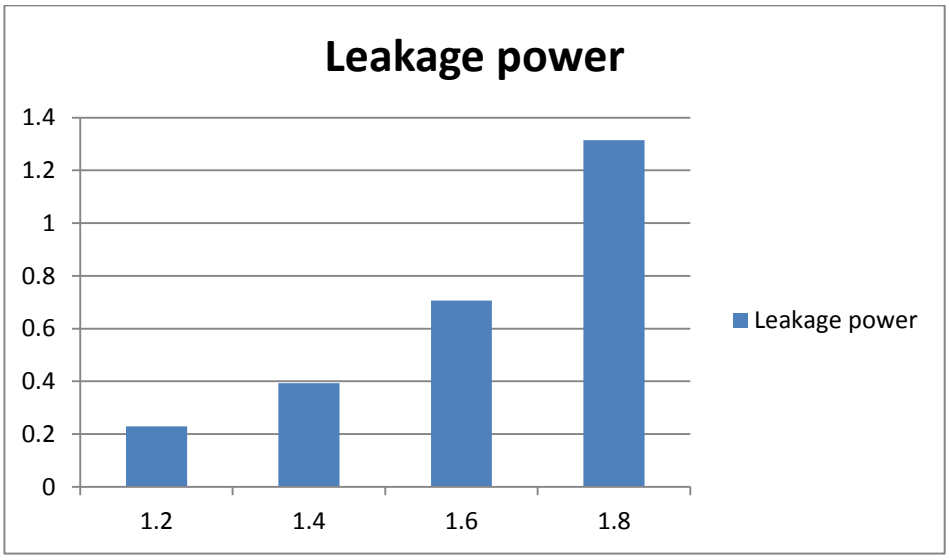

Figure 4 Graph of Leakage power on different level of voltage.

In this graph Leakage Power is rapidly increase with increase in supply voltage. There are increases in supply voltage from 1.2V to 1.4V, 1.6V and 1.8V as the increase in Leakage power are 0.229W, 0.393W, 0.706W and 1.315W respectively.

Table 2 Power dissipation on different value of supply voltage Vccint at 50°C.

Voltage	Leakage Power
1.2	0.585
1.4	1.095
1.6	2.132
1.8	4.487

There is a reduction of 52.48%, 75.59% and 86.96% in leakage power as the voltage is scale down from 1.8V to 1.6V, 1.4V and 1.2V respectively as shown in figure 5 and table 2.In which we have used output load capacitance value is 5pF and clock pulse period is 5ns.

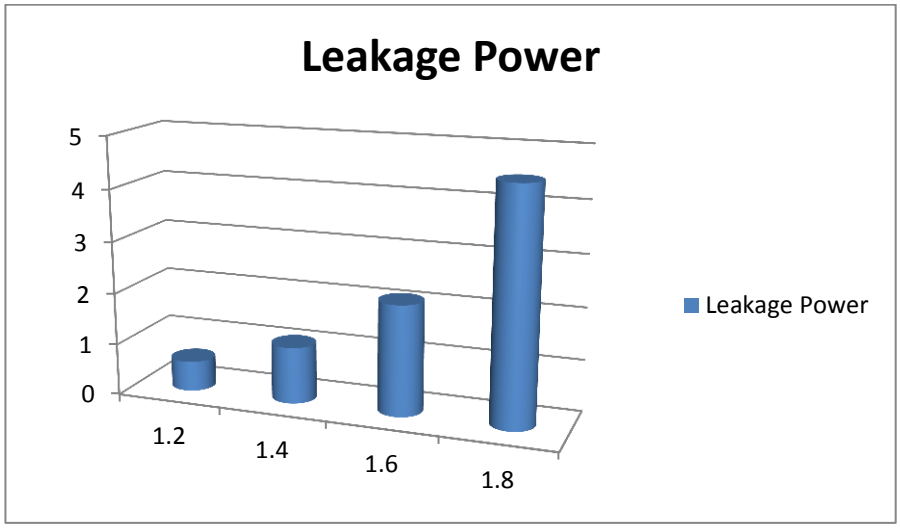

Figure 5 Graph of Leakage power on different level of voltage.

In this graph we have to see that leakage power is rapidly increase with increase in suooly voltage. There are increases in supply voltage from 1.2V to 1.4V, 1.6V and 1.8V as the increase in Leakage power are 0.585W, 1.095W, 2.132W and 4.487W respectively.

Table 3 Power Dissipation on different level of input voltage.

Voltage	Clock power
1.2	0.003
1.4	0.004
1.6	0.005
1.8	0.006

There is a reduction of 46.31%, 70.11% and 82.58% in clock power as the voltage is scale down from 1.8V to 1.6V, 1.4V and 1.2V respectively as shown in figure 6 and table 3.In which we have used output load capacitance value is 5pF and clock pulse period is 5ns.

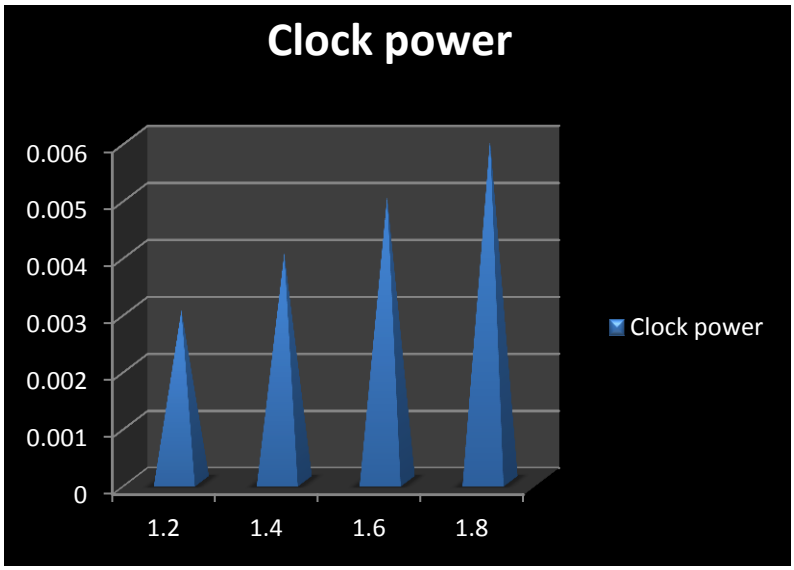

Figure 6 Graph of Clock Power on different level of voltage.

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	9	408,000	1%	
Number used as Flip Flops	9			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	15	204,000	1%	
Number used as logic	15	204,000	1%	
Number using O6 output only	8			
Number using O5 output only	0			
Number using O5 and O6	7			
Number used as ROM	0			
Number used as Memory	0	70,200	0%	
Number used exclusively as route-thrus	0			
Number of occupied Slices	9	51,000	1%	
Number of LUT Flip Flop pairs used	15			
Number with an unused Flip Flop	7	15	46%	
Number with an unused LUT	0	15	0%	
Number of fully used LUT-FF pairs	8	15	53%	
Number of unique control sets	1			
Number of slice register sites lost to control set restrictions	7	408,000	1%	
Number of bonded IOBs	14	600	2%	
Number of RAMB36E1/FIFO36E1s	0	750	0%	
Number of RAMB18E1/FIFO18E1s	0	1,500	0%	
Number of BUFG/BUFGCTRLs	1	32	3%	
Number used as BUFGs	1			
Number used as BUFGCTRLs	0			
Number of IDELAYE2/IDELAYE2_FINEDELAYs	0	700	0%	
Number of ILOGICE2/ILOGICE3/ISERDESE2s	0	700	0%	

Number of ODELAYE2/ODELAYE2_FINEDELAYs	0	650	0%	
Number of OLOGICE2/OLOGICE3/OSERDESE2s	0	700	0%	
Number of PHASER_IN/PHASER_IN_PHYs	0	56	0%	
Number of PHASER_OUT/PHASER_OUT_PHYs	0	56	0%	
Number of BSCANs	0	4	0%	
Number of BUFHCEs	0	168	0%	
Number of BUFRs	0	56	0%	
Number of CAPTUREs	0	1	0%	
Number of DNA_PORTs	0	1	0%	
Number of DSP48E1s	0	1,120	0%	
Number of EFUSE_USRs	0	1	0%	
Number of FRAME_ECCs	0	1	0%	
Number of GTHE2_CHANNELs	0	28	0%	
Number of GTHE2_COMMONs	0	7	0%	
Number of ICAPs	0	2	0%	
Number of IDELAYCTRLs	0	14	0%	
Number of IN_FIFOs	0	56	0%	
Number of MMCME2_ADVs	0	14	0%	
Number of OUT_FIFOs	0	56	0%	
Number of PCIE_3_0s	0	2	0%	
Number of PHASER_REFs	0	14	0%	
Number of PHY_CONTROLs	0	14	0%	
Number of PLLE2_ADVs	0	14	0%	
Number of STARTUPs	0	1	0%	
Number of XADCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.83			

Table 4 Estimated value of slice logic device utilization summary.

4. CONCLUSION

Work is done in order to have an energy efficient traffic light controller design. This will help in designing low power traffic light controller for efficient output.Virtex-7 gives low power readings and so is efficient for designing of not only for traffic light controller but various electronic designs. It is obvious from these tables that at higher value of ambient temperature more power is consumed and vice versa. Through this investigation we are able to design a low power Traffic Light Controller with an efficient output.

5. FUTURE SCOPE

In future, we shall use ultra-scale FPGA for implementation of traffic light controller. These results can be used in future for making efficient Traffic Light Controller on FPGA. It is important to make this useful device efficient and a lot of work can be extended in this field further. We can also use different FPGA families like automotive Artix-7, automotive coolrunner-2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan-3A, automotive Spartan-3E, automotive Spartan-6, Spartan-3, Spartan-3E.

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