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Design of Mobile DDR IO Standards Based Portable Devnagari Unicode Reader on FPGA

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Abstract

Devnagari is used as a script in Hindi, Sanskrit, Marathi, Konkani, Nepali and at least other 18 languages of South Asia. But, no research is available in the field to design portable Devnagari Unicode Reader (DUR). This paper aims to fill this research gap and design a portable DUR as well as make it thermal and energy efficient. Thermal efficient DUR means this DUR is able to operate in the temperature range of 0^{o}C-125^{o}C. Energy efficient DUR means that it would be able to run with the least amount of energy in compare to their traditional counterpart. Four different 28nm 7 Series FPGA and Xilinx ISE 14.6 were taken to verify the energy efficiency and thermal efficiency of a portable Unicode reader using MOBILE DDR input/output standard. Kintex-7 is more thermal efficient than Artix-7. Whereas, Kintex-7 Low Voltage(LV) is even more thermal efficient than general Kintex-7. Artix-7 is energy efficient than Kintex-7. Also, Artix-7 is more energy efficient than Artix-7 LV.

Keywords: Unicode Text Processing, Text Analysis, Text Recognition, Energy Efficiency, Thermal engineering, Devnagari, Temperature.

1 INTRODUCTION

Devnagari is used as a script by Hindi, Sanskrit, Marathi, Konkani, Nepali and at least 18 languages of South Asia. But, no research in Devnagari Unicode Reader(DUR) design has been conducted, which makes this research first of its kind. The aim of this paper is to fill this research gap and design a portable DUR as well as thermal efficient [12] and energy efficient [1,4-11]. Thermal efficient DUR means that DUR is able to operate in the temperature range

of 0ºC-125ºC. Energy efficient DUR means that DUR is able to run with the least amount of energy as compared to their traditional counterpart. DUR is implemented on four different 28nm 7 Series FPGA namely Kintex-7 XC7K70T package, Kintex-7 Low Voltage XC7K70TL package, Artix-7 CSG324 package, Artix-7 Low Voltage CS324L package and Xilinx ISE 14.6 is used to verify the energy efficiency and thermal efficiency of portable Unicode reader using MOBILE DDR [1] input/output standard. Unicode is a universal alphabet. In Muṇḍaka Upanishad, Alphabet or /aḳʃar/ is described as "Like by knowing gold all the gold ornaments could be known, by knowing Akshara, it's another manifestation, the universe is known". This Unicode reader reads the Devnagari Unicode Reader (DUR) and classifies the vowel, consonant, digit and other signs. MOBILE DDR IO standard is used in this DUR to make this more energy efficient and portable. Designers can leverage twice the logic for the same power budget using 28nm Technology in Artix-7 FPGA [2]. Kintex-7 FPGAs are able to provide high signal processing performance and energy efficiency for various applications in Avionics, LED Backlit Flat Panel Displays, 3DTV, LTE Baseband, Portable Ultrasound, Multi-mode Radio, Digital SLR Cameras, and Video on Demand [3]. Kintex-7 FPGA KC705 Evaluation Kit, delivers double the performance using a flexible framework for higher-level systems design that require DDR3, Gigabit Ethernet, PCI Express, and other serial connectivity [3]. In [4], a hybrid software–hardware approach making use of a field-programmable gate array platform as a heat equation solver that can be easily attached to a PC using a PCI bus with the goal of obtaining a portable system to be used during field experiments. According to DVB-S2 standard for LDPC (Low Density Parity Check) codes, a novel LDPC codes encoder circuit structure is designed [5]. Due to the random nature of the input data, this structure significantly reduces the power consumption of the calculation circuit [5]. Using event-triggered radios is well suited and could lead to significant reduction of the overall power consumption of WSNs [6]. Furthermore, proposed solution in [6] is implemented on FPGA to decrease the fabrication cost for low volume applications and make it easier to design, re-use and enhance [6]. The low-power techniques are essential part of VLSI design due to continuing increase in clock frequency and complexity of chip [7]. The power phase measurement system is designed based on FPGA, and the results indicate it almost immune to noise of power [8]. Reference [9] develop power models that consider the effect of logic power, signal power, clock power and I/O power. With the development of technology and usage of FPGA, the power quality detect devices become more and more powerful and the measure accuracy increase quickly [10]. Earlier, the energy efficient Devnagari Unicode Checker is designed with CGVS Approach [11]. CGVS approach is an effective technique in reduction of clock power [11]. In this work, we are working on IO power with means of IO standard. The MOBILE DDR (mDDR) IO standard is also known as LPDDR (Low Power DDR) [13]. The differential outputs are fed into the CK/CK# pins [13], complementary single-ended drivers for outputs, and differential receivers for inputs are used in the differential (DIFF_) version. The advantage of Artix-7 FPGAs are

less investment and minimum power usage. This makes it suitable for mass production applications including: Low Cost Ultrasound, Wireless Backhaul, and Programmable Logic Controller[13]. A port can be exposed as an external port, which is a primary I/O for the whole hardware platform. Port of DUR is shown in red color and block of DUR is shown in green color. In order to avoid transmission line reflection, we have to match impedance of transmission line, port and block using same IO standard for all.

Table 1. Why We Use IO Standard in DUR?

To match impedance of transmission line, port and block		
Impedance of Transmission Line	=	Impedance of Port
Impedance of Block	=	Impedance of Port
Impedance of Transmission Line	=	Impedance of Block

2 MOBILE DDR IO Standard in Unicode Reader

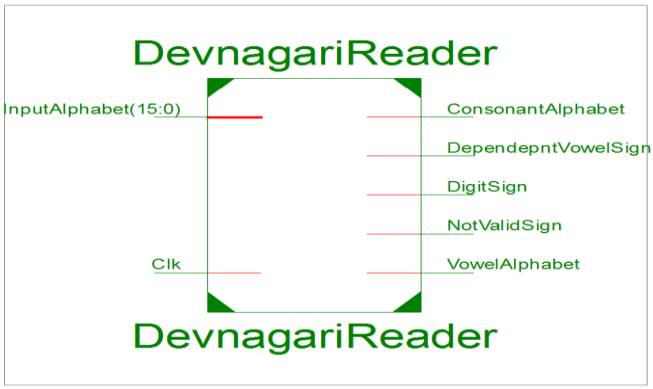

Fig. 1. Top Level Schematic of Devnagari Reader

The top level schematic of DUR is shown in Fig.1. In this implementation of DUR, we used Mobile DDR IO standard from the list of available LVCMOS, SSTL, HSTL, LVDCI, MOBILE DDR and HSUL IO standard in 7 series 28nm FPGA. MOBILE_DDR standard is defined by the JEDEC I/O standard JESD209A [13]. It is a 1.8V single-ended I/O standard that doesn't require VREF and VTT voltage supplies [13]. 7-series-FPGAs support mDDR input/output standard for single-ended signaling and differential outputs [13].

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3 Power Usage In Unicode Reader

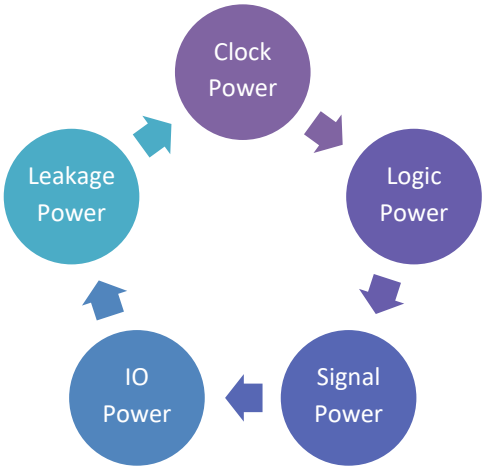

Fig. 2. Different Component of Power

Depending on the state of device, we can classify power Usage into broadly three types, which are discussed further.

3.1 Dynamic Power Usage

The power Usage when DUR is in ON state is called dynamic power ($P_{D)}$, It consists of BRAM Power, Clock Power(CP), DSP Power, IO Power (IOP), Logic Power(LP), and Signal Power(SP) and. CP, LP, IOP and SP are compulsory in any design on FPGA. BRAM power is consumed when we implement Memory, whereas DSP power consumes with Filter on FPGA.

Table 2. Component of Dynamic Power

Circuit	Common Power	Special Power
Any Circuit	CP, LP, SP, IOP	----------
Memory Circuit	CP, LP, SP, IOP	BRAM Power
Filter Circuit	CP, LP, SP, IOP	DSP Power

Dynamic power is directly proportional to load capacitance, supply voltage and frequency.

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Table 3. Parameter of Dynamic Power

parameter	Intermediate Value	Range
Frequency	25GHz,125GHz, 625GHz	5 GHz-1THz
Capacitance	5pF	0pF-1000nF
Voltage	1.0V, 0.9V, 1.8V, 1.7V	0V-5V

We operated our DUR with an initial frequency of 5GHz, and maximum frequency of 1 THz along with providing intermediate frequency of 25GHz, 125GHz and 625GHz. We are taking 5pF initial capacitance, 1.0V supply voltage for Artix-7 and Kintex-7 and 0.9V for Artix-7 Low Voltage and Kintex-7 Low Voltage.

3.2 Static Power Usage

Static Power (P_s) is the power Usage, when device is in off state. It is also called Quiescent power, which depends on the Quiescent current flow in the device. We can calculate the static power by using formula $P_s = V_{DD} * I_{Leak}$

3.3 Junction Temperature of FPGA

Junction Temperature depends on the leakage power or current flow in the design on FPGA. Quiescent power is related to the ambient temperature of the design. Ambient temperature is the temperature of the surrounding of the design. In this work, the junction temperature is taken to be constant 25 ^oC.

3.4 Power Usage and Junction Temperature in Artix-7

Table 4. Power Usage on Different Device Operating Frequency

Power	5GHz	25GHz	125GHz	625GHz	1THz
Clock	0.027	0.135	0.674	3.369	5.390
Logic	0.001	0.002	0.008	0.036	0.057
Signal	0.004	0.022	0.108	0.539	0.863
IOs	0.090	0.394	1.912	9.501	15.193
Leak-age	0.083	0.084	0.094	0.291	0.812
Total	0.205	0.637	2.796	13.736	22.315

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In Table 4, there is 99.49%, 98.25%, 99.54%, 99.41% and 89.78% saving in CP, LP, SP, IOP, and leakage power when we scale down the operating frequency from 1THz to 5 GHz.

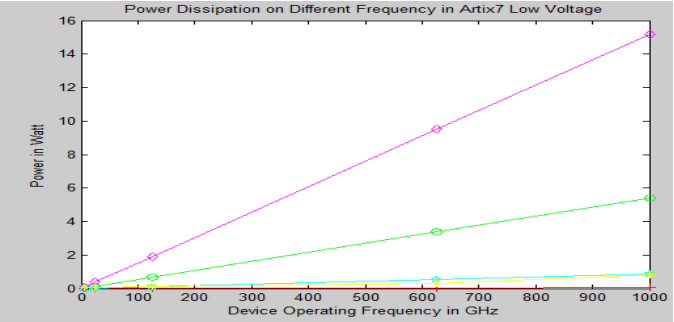

Fig. 3 Plot of Power and Frequency in Matlab

The Graph shown in Fig.3 is created using the Matlab script as shown in Fig.4. The Y-axis shows the Power Usage in Watt and X-axis is the operating frequency in GHz. In Fig.3, red line shows LP, green line shows CP, cyan line shows the SP, magenta shows the IOP and yellow line depicts the leakage power.

JuncTempArtix7.m

```
%Junction Temperature on Different Device Operating Frequency
x=[5 25 125 625 1000];
Clock=[0.027    0.135    0.674    3.369    5.390];
Logic=[0.001    0.002    0.008    0.036    0.057];
Signal=[0.004    0.022    0.108    0.539    0.863];
IOs=[0.090  0.394    1.912    9.501    15.193];
Leakage=[0.083  0.084    0.094    0.291    0.812];
plot(x,Clock,'g',x,Clock,'go');
hold on;
plot(x,Logic,'r',x,Logic,'r+');
hold on;
plot(x,Signal,'c',x,Signal,'cp');
hold on;
plot(x,IOs,'m',x,IOs,'md');
hold on;
plot(x,Leakage,'y',x,Leakage,'y*');
xlabel('Device Operating Frequency in GHz')
ylabel('Power in Watt')
title('Power Dissipation on Different Frequency in Artix7 Low Voltage');
```

Fig. 4 Matlab Script of Power and Frequency in Matlab

In Table 5, there is 54.76% saving in junction temperature when we scale the operating frequency from 1THz to 5 GHz.

Table 5. Junction Temperature on Different Device Operating Frequency

Temperature	5GHz	25GHz	125GHz	625GHz	1THz
Junction Temperature	25.2	25.4	26.4	31.3	55.7

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3.5 Power Usage on Artix-7 Low Voltage

Table 6. Power Usage on Different Device Frequency

Power	5GHz	25GHz	125GHz	625GHz	1THz
Clock	0.031	0.155	0.777	3.886	6.218
Logic	0.001	0.002	0.008	0.034	0.054
Signal	0.005	0.024	0.117	0.584	0.935
IOs	0.089	0.386	1.873	9.309	14.885
Leak-age	0.078	0.079	0.086	0.244	0.629
Total	0.203	0.646	2.867	14.057	22.721

In Table 6, there is 99.50%, 98.15%, 99.41%, 99.40% and 87.6% saving in CP, LP, SP, IOP, and leakage power when we scale down the operating frequency from 1THz to 5 GHz.

Table 7. Junction Temperature on Different Device Frequency

Temperature	5GHz	25GHz	125GHz	625GHz	1THz
Junction Temperature	25.9	28.0	38.2	89.7	125

In Table 7, there is 54.76% saving in junction temperature when we scale operating frequency from 1THz to 5 GHz.

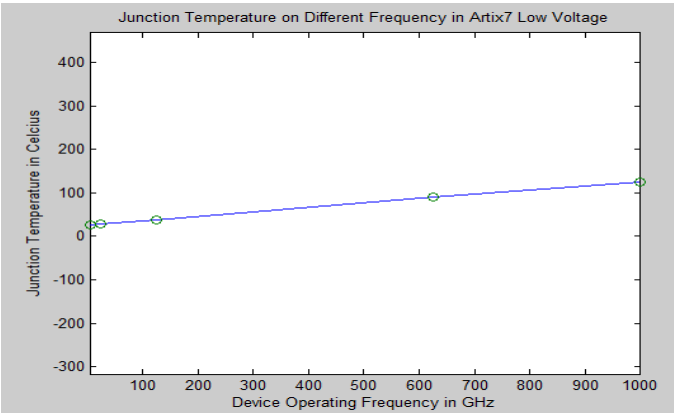

Fig. 5. Plot of Junction Temperature and Frequency in Matlab

Graph shown in Fig.5 is created by the Matlab script shown in Figure 6. The Y-axis represents the junction temperature in Celsius and X-axis shows the operating frequency in GHz.

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```
JuncTempArtix7.m
1   %Junction Temperature on Different Device Operating Frequency
2 - x=[5 25 125 625 1000];
3 - y=[25.9 28.0 38.2 89.7 125];
4 - plot(x,y,x,y,'o');
5 - axis('equal')
6 - xlabel('Device Operating Frequency in GHz')
7 - ylabel('Junction Temperature in Celcius')
8 - title('Junction Temperature on Different Frequency in Artix7 Low Voltage');
```

Fig. 6. Matlab Script of Power and Frequency in Matlab

4 COMPARISON OF DIFFERENT FPGA

4.1 Comparison of Different FPGA on 25GHz

Table 8. Power Usage on Different FPGA

Power	Artix-7	Kintex-7 LV	Artix-7 LV	Kintex-7
Clock	0.135	0.136	0.155	0.191
Logic	0.002	0.002	0.002	0.002
Signal	0.022	0.019	0.024	0.021
IOs	0.394	0.386	0.386	0.394
Leakage	0.084	0.074	0.079	0.081
Total	0.637	0.618	0.646	0.689

There is no variation in LP, when we use various FPGA. Also, there is no change in IOP with general Artix-7 and Kintex-7 and no change in IOP with Low Voltage Artix-7 and Low Voltage Kintex-7 is seen.

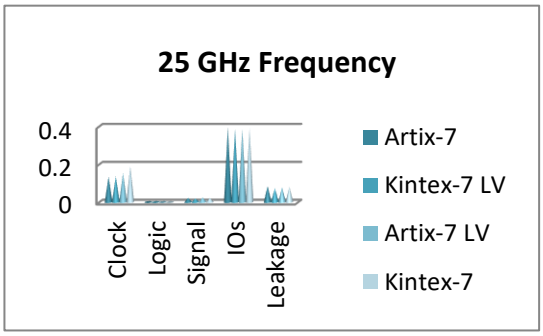

Fig. 7. Power in Watt on 25 GHz Device Frequency

IOP is maximum in comparison to other dynamic power. CP is the highest in Kintex-7 and lowest in Artix-7. Whereas, SP is minimum in Kintex-7 Low Voltage and maximum with Artix-7 Low Voltage. Also, leakage power is the lowest in Kintex-7 Low Voltage among all these four available FPGA.

Table 9. Junction Temperature on Different FPGA

FPGA	Artix-7	Kintex-7 LV	Artix-7 LV	Kintex-7
Junction Temperature	27.9	26.3	28.0	26.4

Junction Temperature is the maximum with Artix-7 Low Voltage FPGA. It is minimum with Kintex-7 Low Voltage.

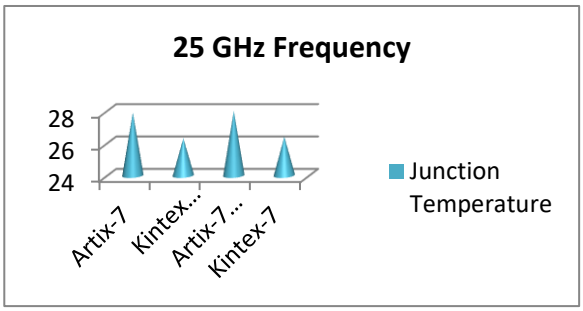

Fig. 8. Junction Temperature For 25 GHz Device Frequency

4.2 Comparison of Different FPGA on 625GHz

Table 10. Power Usage on Different FPGA

Power	Artix-7	Kintex-7 LV	Artix-7 LV	Kintex-7
Clock	3.369	3.411	3.886	4.773
Logic	0.036	0.034	0.034	0.033
Signal	0.539	0.475	0.584	0.530
IOs	9.501	9.309	9.309	9.501
Leakage	0.291	0.109	0.244	0.140
Total	13.736	13.337	14.057	14.977

When operating frequency is 625GHz, then there is 29.42% saving in CP, when we are using Artix-7 FPGA in place of Kintex-7 FPGA as shown in Table 10.

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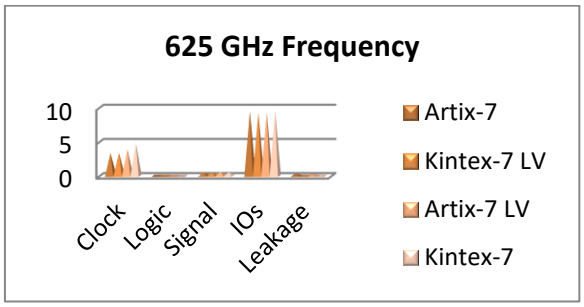

Fig. 9. Power in Watt on 625 GHz Device Frequency

When operating frequency is 625GHz, then there is 18.66% saving in SP, when we are using Artix-7 LV FPGA in place of Kintex-7 FPGA as shown in Table 10. On similar device frequency, there is 8.33% saving in LP, when we use Kintex-7 FPGA in place of Artix-7 FPGA as shown in Table 10.

Table 11. Junction Temperature on Different FPGA

FPGA	Artix-7	Kintex-7 LV	Artix-7 LV	Kintex-7
Junction Temperature	88.2	52.4	89.7	55.7

There is 41.58% saving in junction temperature with Kintex-7 LV FPGA in compare to Artix-7 LV FPGA.

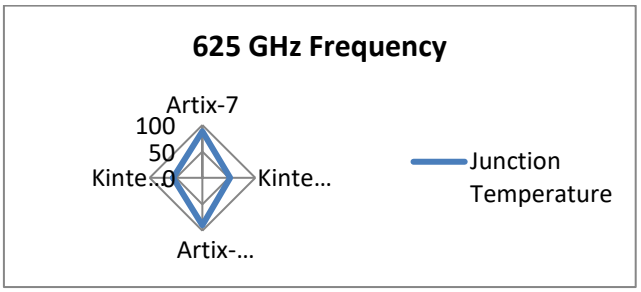

Fig. 10. Junction Temperature For 625 GHz Device Frequency

4.3 Comparison of Different FPGA on 1THz

Table 12. Power Usage on Different FPGA

Power	Artix-7	Kintex-7 LV	Artix-7 LV	Kintex-7
Clock	5.390	5.458	6.218	7.637

Logic	0.057	0.054	0.054	0.053
Signal	0.863	0.759	0.935	0.847
IOs	15.193	14.885	14.885	15.193
Leakage	0.812	0.159	0.629	0.232
Total	22.315	21.315	22.721	23.962

There is 2.04% saving in IOP dissipation with both Kintex-7 and Artix-7 LV FPGA as compared to general Artix-7 and Kintex-7 FPGA.

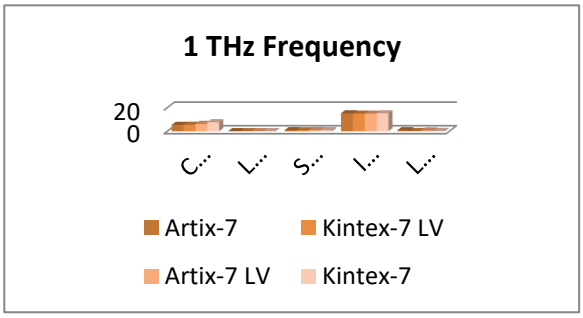

Fig. 11. Power in Watt on 1 THz Operating Frequency

Also, there is 80.42% saving in leakage power with Kintex-7 Low Voltage FPGA than Artix-7 FPGA. There is 11.05% saving in the total power consumption with Kintex-7 LV FPGA in comparison to Kintex-7 FPGA as shown in Table 12.

Table 13. Junction Temperature on Different FPGA

FPGA	Artix-7	Kintex-7 LV	Artix-7 LV	Kintex-7
Junction Temperature	125	68.7	125	74.1

Artix-7 is the worst heat producer that results in the highest junction temperature. There is 45.04% saving in junction temperature with any Kintex-7 in comparison to either Artix-7 and Artix-7 LV.

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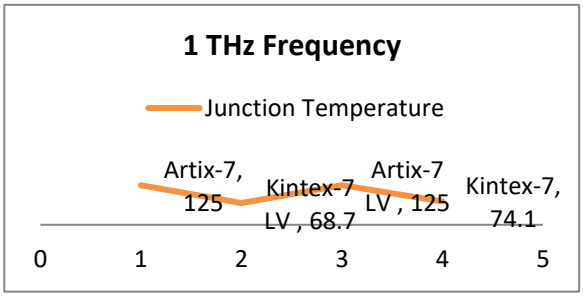

Fig. 12. Junction Temperature For 1 THz Device Frequency

5 Conclusion

It is a thermal efficient DUR because it is able to operate in the temperature range of 0^{o}C-125^{o}C. It is energy efficient DUR too because it runs with the least amount of energy in compare to their traditional counterpart Kintex-7 is more thermal efficient than Artix-7. Whereas, Kintex-7 Low Voltage (LV) is even more thermal efficient than general Kintex-7. Artix-7 is more energy efficient than Kintex-7 and Artix-7 LV FPGA. Artix-7 is the worst heat producer that result in the highest junction temperature. Kintex-7 Low Voltage is dissipating minimum leakage power. The usage of Mobile DDR IO Standard enhance portability in DUR design**.** There is 99.50%, 98.15%, 99.41%, 99.40% and 87.6% saving in CP, LP, SP, IOP, and leakage power, when we scale down the operating frequency from 1THz to 5 GHz on Atrix-7 FPGA.

6 Future Scope

By using Mobile DDR IO Standard, we can also design both energy efficient and thermal efficient FIR Guassian low Pass Filter, Image ALU, Memory Interface, ALU, Fibonacci Generator, Frame Buffer, ITC'99-b01 Benchmark Circuit, Multiplexer, Bi-Directional VCM, Parallel Integrator, Voltage Based Fire Sensor, Frequency Meter, Counter, Register, Fire Sensor, Image Inverter, GCD, Bengali Unicode Reader, and UART etc. We can also extend this work for various Unicode scripts like Arabic, Roman, Mandarin etc. We can use different FPGA for implementation of this Unicode reader like LatticeECP FPGA, Spartan-6 FPGA, Cyclone FPGA, Speedster FPGA, SiliconBlue's FPGA etc.

REFERENCES

1. Kumar, T., Pandey, B., Das, T., & Chowdhry, B. S. (2014). Mobile DDR IO Standard Based High Performance Energy Efficient Portable ALU Design on FPGA. *Wireless Personal Communications*, *76*(3), 569-578.

2. Artix-7 FPGA Family, xilinx.com/publications/prod_mktg/Artix-7-Product-Brief.pdf (Last visited on 14th may 2014)
3. Kintex-7 FPGA Family, http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/ (last visited on 14th may 2014)
4. Pardo, F., López, P., Cabello, D., & Balsi, M. (2010). FPGA computation of the 3D heat equation. *Computational Geosciences*, *14*(4), 649-664.
5. Zou, X., Qian, H., & Cheng, S. (2012). FPGA Design and Implementation of Low Power Consumption LDPC Encoder Based on DVB-S2. In *Advances in Computer, Communication, Control and Automation* (pp. 85-92). Springer Berlin Heidelberg.
6. Jean-François, P., Jean-Jules, B., & Yvon, S. (2013). Modeling, design and implementation of a low-power FPGA based asynchronous wake-up receiver for wireless applications. *Analog Integrated Circuits and Signal Processing*, *77*(2), 169-182.
7. Kathuria, J., Khan, M. A., Abraham, A., & Darwish, A. (2014). Low Power Techniques for Embedded FPGA Processors. In *Embedded and Real Time System Development: A Software Engineering Perspective* (pp. 283-304). Springer Berlin Heidelberg.
8. Zhang, X., Zhang, Y., & Lu, X. (2012). Phase Measurement of Three-Phase Power Based on FPGA. In *Wireless Communications and Applications* (pp. 170-179). Springer Berlin Heidelberg.
9. Deng, L., Sobti, K., Zhang, Y., & Chakrabarti, C. (2011). Accurate area, time and power models for FPGA-based implementations. *Journal of Signal Processing Systems*, *63*(1), 39-50.
10. Chen, X., & Zhang, Y. (2012). Detection and Analysis of Power System Harmonics Based on FPGA. In *Wireless Communications and Applications* (pp. 445-454). Springer Berlin Heidelberg.
11. Teerath Das, Tanesh Kumar, S. M. Mohaiminul Islam, Bishwajeet Pandey, Md Atiqur Rahman and Mahbub-E-Noor, "Low Power Devnagari Unicode Checker Design Using CGVS Approach", "Advanced Materials Research", ISSN:1022-6680 (print version), ISSN:1662-8985 (electronic Version), Trans Tech Publications, Switzerland, Indexed by Elsevier: **SCOPUS** (Accepted)
12. Bishwajeet Pandey, Tanesh Kumar, Teerath Das and Jagdish Kumar " Thermal Mechanics Based Energy Efficient FIR Filter for Digital Signal Processing", Applied Mechanics and Materials (AMM) Journal, ISSN:1662-7482(online version), ISSN:1660-9336(print version), Trans Tech Publications, Switzerland, Indexed by Elsevier: **SCOPUS** (Accepted)
13. 7 Series FPGA SelectIO Resources User Guide UG361 (v1.4) June 21, 2013http://japan.xilinx.com/support/documentation/user_guides/ug471_7Series_SelectIO.pdf