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LVCMOS and BLVDS Based Energy Efficient Counter Design on 28nm FPGA

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***Abstract*—Counter play an important role in design of stopwatch, countdown of space craft, rocket, launcher and so on. In this work, we are going to design energy efficient counter. For that we are exploring 10 different configuration of counter and find the most energy efficient counter among them. For further reduction of power dissipation of the most efficient counter, we are using different Input/Output standards and select the most energy efficient IO standards for counter. 8 bit Up counter with Load has maximum reduction in total power among 10 different counters. When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 65-81% reduction in total power dissipation in 8 bit Up counter with Load. As we move down the column from LVCMOS15 to LVCMOS33 there is 94-77% reduction in IO power Dissipation and leakage power variation is very less.**

***Keywords*—Counter, LVCMOS, BLVDS, FPGA, Energy Efficient, clock, enable, up down counter, one hot counter, random LFSR counter, divide by 3 counter.**

I. INTRODUCTION

BLVDS is bus low-voltage differential signaling. BLVDS provides new approach to fast interfaces across cables. LVCMOS is a low voltage complementary oxide semiconductor, it is one of the CMOS technology. In this paper the energy efficient counter has been designed based on BLVDS and LVCMOS technology. We have used LVCMOS15, LVCMOS18, LVCMOS25, LVCMOS33 and BLVDS_25 at frequency 1GHz.

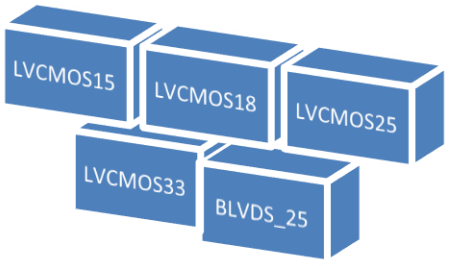

Figure 1: IO TECHNIQUES USED

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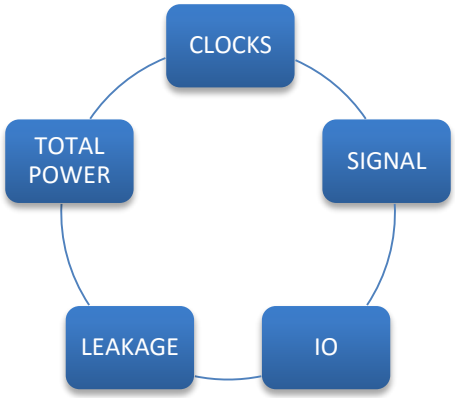

Figure 2: TYPES OF POWER DISSIPATION

The total power dissipation in BLVDS_25 is maximum in nine counters – divide by 4.5, gray counter, 8 bit simple up counter, 8 bit up counter with load, up down counter, one hot counter, random LFSR counter, LFSR up/down counter and divide by 3 counter.

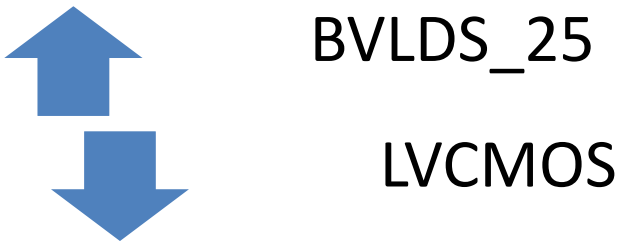

Figure 3: TOTAL POWER DISSIPATION FOR 9 COUNTERS

But in divide by 2 counter the LVCMOS33 has maximum total power dissipation.

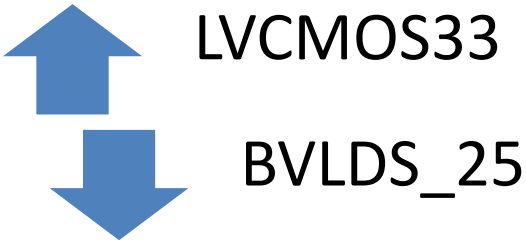

Figure 4: **TOTAL POWER DISSIPATION FOR DIVIDE BY 2 COUNTER**

A counter is a set of flip-flops and is used to count pulses. A counter can be used as frequency divider, for example divide by 2 counter, divide by 3 counter, divide by 4.5 counter and many more. In asynchronous counters the output of first flip-flop is connected with input of second flip-flop and so on. Synchronous counters are those counters in which there is no connection between the output of first flip-flop and clock input of next flip-flop and so on.

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II. SCHEMATICS OF DIFFERENT COUNTERS

A. Divide By 4.5 Counter

Divide by 4.5 Counter generates two symmetrical pulses for every 9 clocks as shown in Figure 1. Duty cycle for above generated clock is 40% and it ensures glitch-free output.

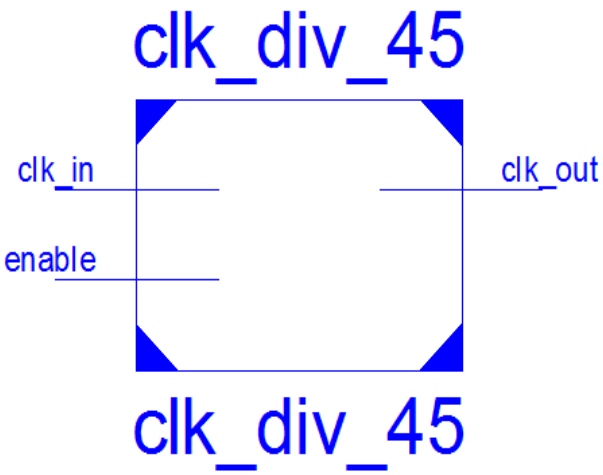

Figure 5: DIVIDE BY 4.5 COUNTER

B. Gray Counter

Gray counter uses gray code in which there is difference of only one bit between successive states as shown in Figure 2. 8 bit gray counter requires 3 flip flops and starts its counting with 000 and proceed to 001,011,010,110,111,101,100 and then reset to 000.

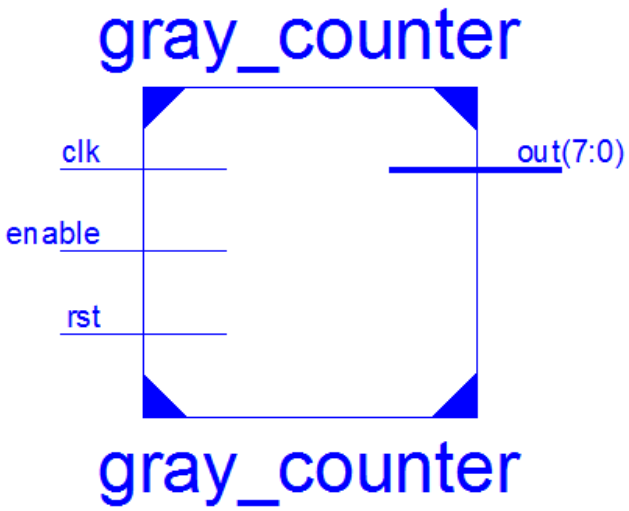

Figure 6: GRAY COUNTER

C. Divide by 2 Counter

Divide by 2 Counter divides the frequency by 2 and time period becomes double as shown in Figure 3. It can also be use if we want to shift bits to right e.g. if we want to convert 1010 to 0101 then we can use this counter.

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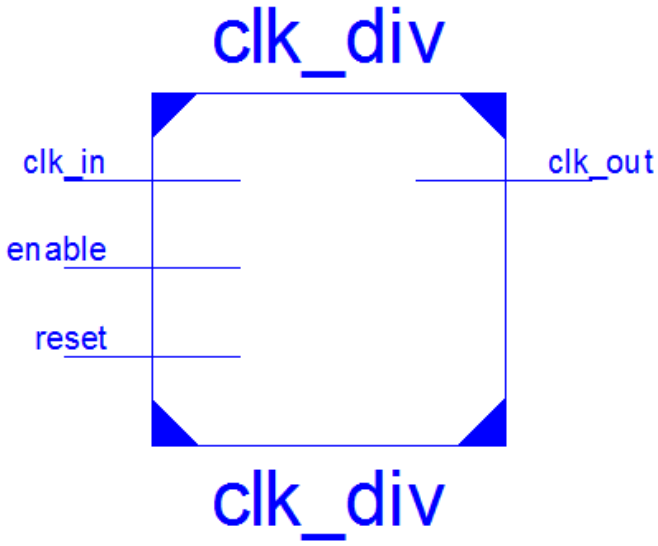

Figure 7: DIVIDE BY 2 COUNTER

D. 8 Bit Simple Up Counter

When reset is pressed then the counter is set to 0 and when it is enabled then every time it is incremented by one till it counts 111 as shown in figure 4.

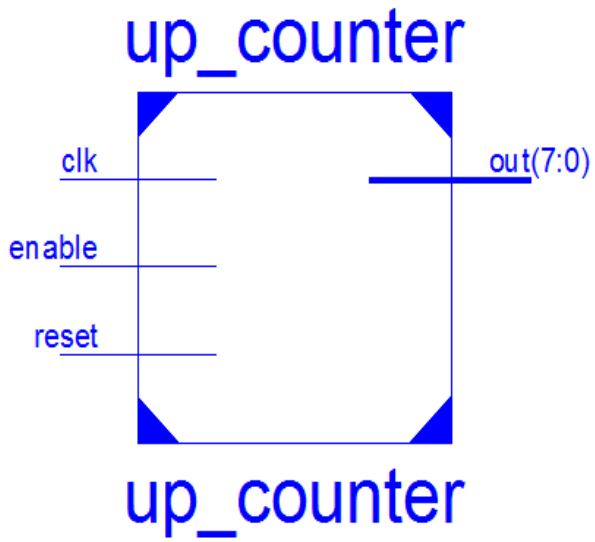

Figure 8: SIMPLE UP COUNTER

E. Up Counter with Load

When Up counter with load is reset then the counter is set to 0. When load is 1 then count will start from data. If data is 3 then count start with 3 and with every enable count will increment i.e. 3->4->5->6->7->0. If load is 0 then this counter become simple up down counter as shown in Figure 5.

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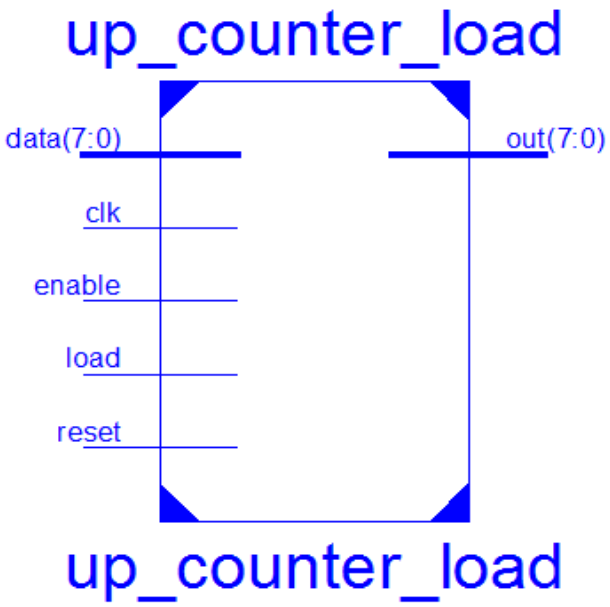

Figure 9: UP COUNTER WITH LOAD

F. Up Down Counter

When reset is active high then the counter is set to 0 and when up_down button is pressed then there is increment of one every time and if up_down button is not active then there is decrement of one as shown in Figure 6.

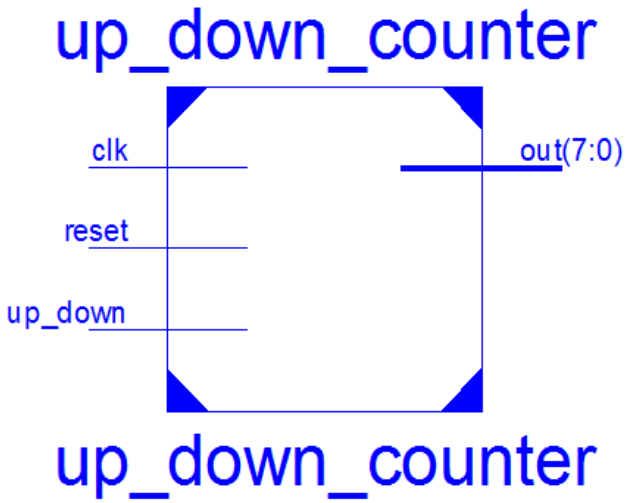

Figure 10: UP DOWN COUNTER

G. One Hot Counter

The one hot counter counts in such a way that one bit is high and all other bits are low. This counter does not need any decoder. When nth bit is high that means the counter is in the nth state as shown in figure 7.

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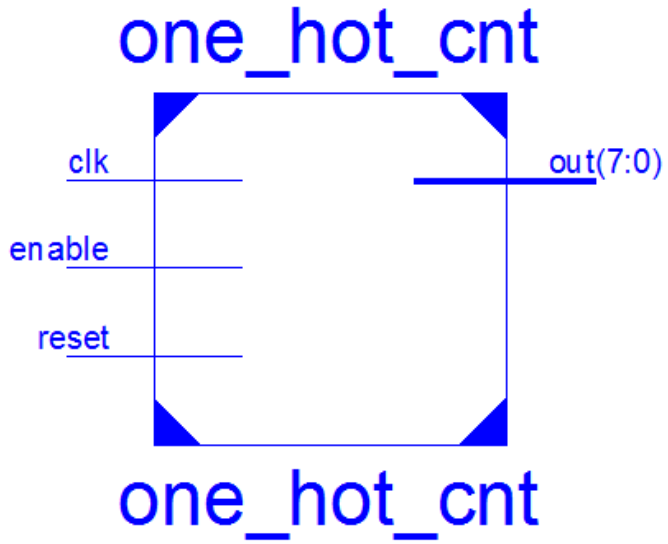

Figure 11: ONE HOT COUNTER

H. LFSR Counter

LFSR is a linear feedback shift register counter with XOR gates and generates random numbers. Eg, in 8 bit counter, say the output of 7pin and 3pin is XNOR to get the 8th bit .

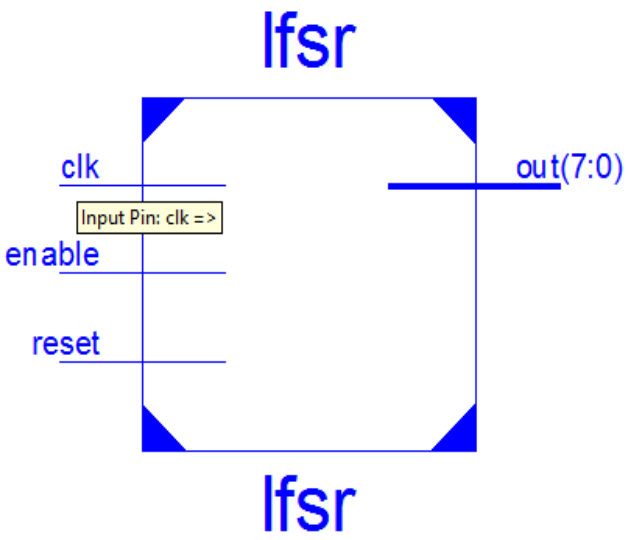

Figure 12: LFSR COUNTER

I. LFSR Up Down

LFSR is used for random number generation. When it is used as counter, output of LFSR counter reset to any random number. In general counter, counter always reset to 0. LFSR UP Down is also differ with simple LFSR because it consider the extreme case of overflow as shown in Figure 9.

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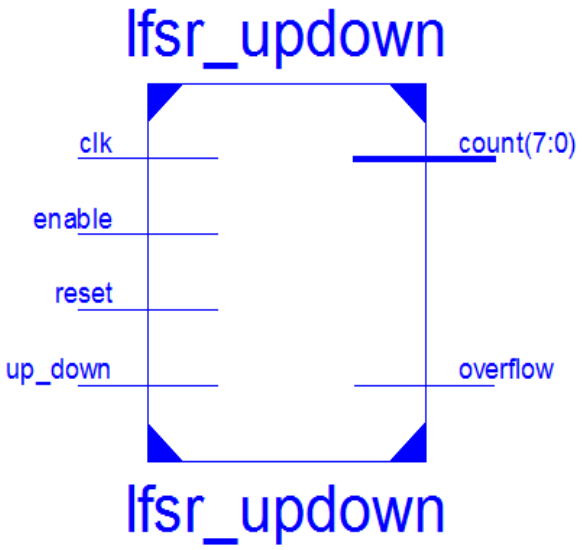

Figure 13: LFSR UP DOWN

J. Divide By 3 Counter

Divide by 3 counter divides the frequency by 3.When reset is active high that means counter is set to 0 and output is 0,1 or 2.

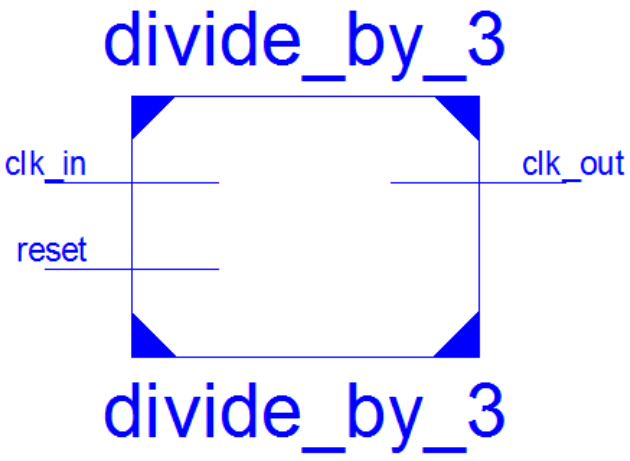

Figure 14: DIVIDE BY 3 COUNTER

III. RELATED WORK

LVCMOS IO standard is used to design energy efficient bidirectional visitor counter machine [1]. Our work is not limited to one counter, we have used ten counters. LVCMOS IO standard is used to design counters with LVCMOS15, LVCMOS18, LVCMOS33 whereas in this paper we have also used LVCMOS25 along with LVCMOS15, LVCMOS18 and LVCMOS33 [2].Also we have included one more technique. LVCMOS IO standard technique is used to make energy efficient Gurmukhi Unicode reader. But we are using this technique to make energy efficient counters [3]. The mapping technique is used to make energy efficient counters whereas we have used

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LVCMOS and BVLDS techniques [4]. LVCMOS technique is also used to design energy efficient Vedic multiplier [5]

IV. RESULTS

Table 1: DIVIDE BY 4.5 COUNTER

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.006	0.001	0.037	0.044	0.089
LVCMOS15	0.006	0.001	0.004	0.042	0.054
LVCMOS18	0.006	0.001	0.005	0.042	0.055
LVCMOS25	0.006	0.001	0.007	0.043	0.058
LVCMOS33	0.006	0.001	0.012	0.044	0.064

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 39.32%, 38.20%, 34.83% and 28.08% reduction in total power dissipation respectively as shown in Table 1. As we move down the column from LVCMOS15 to LVCMOS33 there is 89.18%, 86.48%, 81.08% and 67.56% reduction in IO power Dissipation respectively and leakage power variation is very less.

Table 2: GRAY COUNTER

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.005	0.001	0.294	0.045	0.346
LVCMOS15	0.005	0.001	0.035	0.042	0.083
LVCMOS18	0.005	0.001	0.047	0.043	0.096
LVCMOS25	0.005	0.001	0.084	0.043	0.133
LVCMOS33	0.005	0.001	0.143	0.044	0.194

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 76.01%, 72.25%, 61.56% and 43.93% reduction in total power dissipation respectively as shown in Table 2. As we move down the column from LVCMOS15 to LVCMOS33 there is 88.09%, 84.01%, 71.42% and 51.36% reduction in IO power Dissipation respectively and leakage power variation is very less.

Table 3 : DIVIDE BY 2 COUNTER

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.005	0.000	0.049	0.044	0.099
LVCMOS15	0.005	0.000	0.022	0.042	0.069
LVCMOS18	0.005	0.000	0.029	0.042	0.077
LVCMOS25	0.005	0.000	0.051	0.043	0.100
LVCMOS33	0.005	0.000	0.087	0.044	0.137

When we use BLVDS_25, LVCMOS15, LVCMOS18, LVCMOS25, and in place of LVCMOS33 then there is 27.73%, 49.63%, 43.79% and 27% reduction in total power dissipation respectively as shown in Table 3. As we move down the column from BLVDS_25 to LVCMOS25 there is 43.67%, 74.71%, 66.66% and 41.37% reduction in IO power dissipation respectively and leakage power variation is very less.

Table 4 : 8 BIT SIMPLE UP COUNTER

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.005	0.001	0.299	0.045	0.350
LVCMOS15	0.005	0.001	0.041	0.042	0.090

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LVCMOS18	0.005	0.001	0.056	0.043	0.105
LVCMOS25	0.005	0.001	0.101	0.043	0.150
LVCMOS33	0.005	0.001	0.173	0.044	0.223

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 74.28%, 70%, 57.14% and 36.28% reduction in total power dissipation respectively as shown in Table 4. As we move down the column from LVCMOS15 to LVCMOS33 there is 86.28%, 81.27%, 66.22% and 42.14% reduction in IO power dissipation respectively and leakage power variation is very less.

Table 5 : 8 BIT UP COUNTER WITH LOAD

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.005	0.001	0.282	0.045	0.333
LVCMOS15	0.005	0.001	0.017	0.042	0.065
LVCMOS18	0.005	0.001	0.022	0.042	0.071
LVCMOS25	0.005	0.001	0.038	0.043	0.087
LVCMOS33	0.005	0.001	0.064	0.044	0.114

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 80.48%, 78.67%, 73.87% and 65.76% reduction in total power dissipation respectively as shown in Table 5. As we move down the column from LVCMOS15 to LVCMOS33 there is 93.97%, 92.19%, 86.52% and 77.30% reduction in IO power dissipation respectively and leakage power variation is very less.

Table 6 : UP-DOWN COUNTER

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.005	0.001	0.294	0.045	0.346
LVCMOS15	0.005	0.001	0.034	0.042	0.083
LVCMOS18	0.005	0.001	0.047	0.043	0.095
LVCMOS25	0.005	0.001	0.083	0.043	0.133
LVCMOS33	0.005	0.001	0.142	0.044	0.193

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 76.01%, 72.54%, 61.56% and 44.21% reduction in total power dissipation respectively as shown in Table 6. As we move down the column from LVCMOS15 to LVCMOS33 there is 88.43%, 84.01%, 71.76% and 51.70% reduction in IO power Dissipation respectively and leakage power variation is very less.

Table 7 : ONE HOT COUNTER

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.005	0.001	0.287	0.045	0.338
LVCMOS15	0.005	0.001	0.024	0.042	0.072
LVCMOS18	0.005	0.001	0.033	0.042	0.081
LVCMOS25	0.005	0.001	0.059	0.043	0.107
LVCMOS33	0.005	0.001	0.100	0.044	0.150

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 78.69%, 76.03%, 68.34% and 55.62% reduction in total power dissipation respectively as shown in Table 6. As we move down the column from

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LVCMOS15 to LVCMOS33 there is 91.63%, 88.50%, 79.44% and 65.15% reduction in IO power dissipation respectively and leakage power variation is very less.

Table 8 : RANDOM LFSR COUNTER

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.005	0.001	0.298	0.045	0.349
LVCMOS15	0.005	0.001	0.040	0.042	0.089
LVCMOS18	0.005	0.001	0.055	0.043	0.103
LVCMOS25	0.005	0.001	0.098	0.043	0.147
LVCMOS33	0.005	0.001	0.168	0.044	0.218

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 74.49%, 70.48%, 57.87% and 37.53% reduction in total power dissipation respectively as shown in Table 6. As we move down the column from LVCMOS15 to LVCMOS33 there is 86.57%, 81.54%, 67.11% and 43.62% reduction in IO power Dissipation respectively and leakage power variation is very less.

Table 9 : LFSR UP DOWN COUNTER

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.006	0.001	0.332	0.045	0.384
LVCMOS15	0.006	0.001	0.040	0.042	0.090
LVCMOS18	0.006	0.001	0.054	0.043	0.104
LVCMOS25	0.006	0.001	0.097	0.043	0.148
LVCMOS33	0.006	0.001	0.167	0.044	0.218

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 76.56%, 72.91%, 61.45% and 43.22% reduction in total power dissipation respectively as shown in Table 9. As we move down the column from LVCMOS15 to LVCMOS33 there is 87.955%, 83.73%, 70.78% and 49.69% reduction in IO power Dissipation respectively and leakage power variation is very less.

Table 10 : DIVIDE BY 3

	CLOCKS	SIGNAL	IO	LEAKAGE	TOTAL
BLVDS_25	0.005	0.000	0.036	0.044	0.086
LVCMOS15	0.005	0.000	0.003	0.042	0.050
LVCMOS18	0.005	0.000	0.004	0.042	0.051
LVCMOS25	0.005	0.000	0.005	0.043	0.054
LVCMOS33	0.005	0.000	0.008	0.044	0.057

When we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 41.86%, 40.69%, 37.20% and 33.72% reduction in total power dissipation respectively as shown in Table 10. As we move down the column from LVCMOS15 to LVCMOS33 there is 91.66%, 88.88%, 86.11% and 77.77% reduction in IO power Dissipation respectively and leakage power variation is very less.

V. CONCLUSION

8 bit up counter is the most energy efficient counter among the nine other counters we have used. In most of the counters, nine out of ten counters, BLVDS IO technique uses more power than LVCMOS. LVCMOS is better IO technique. In all the counters variation in leakage power is very less. In divide by 4.5 counter when we use LVCMOS15, LVCMOS18, LVCMOS25, and LVCMOS33 in place of BLVDS_25 then there is 28%-39% reduction in total power dissipation. Similarly, in gray counter reduction in total dissipation is 43%-76%, in 8 bit simple up counter it is 36%-74%, in

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up counter 65%-80%, up down counter 44%-76%,one hot counter 55%-78%, random LFSR counter 37%-74%, LFSR up down counter 43%-77%,random LFSR counter 33%-42%,divide by 3 counter 33%-42%. But in divide by 2 counter, when we use BLVDS_25, LVCMOS15, LVCMOS18, LVCMOS25, and in place of LVCMOS33 then there is 27%-49% reduction in total power dissipation.

VI. FUTURE SCOPE

In this work of energy efficient counter design, we are using two different IO standards LVCMOS and BLVDS. In future, we can redesign these counters and also make it energy efficient using other IO standards like SSTL, HSTL, LVDCI, HSUL, Mobile DDR, PCI, GTL and so on. Here, frequency is constant. There is open scope to redesign these counter using frequency scaling, capacitance scaling, voltage scaling and other energy efficient techniques. In this work, verilog is used as hardware description language. In future, we can redesign these counters using other HDL like VHDL, SystemC, System Verilog and so on.

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