

SSTL I/O Standard based Simulation of Energy Efficient VCM on FPGA

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Abstract— In this paper SSTL I/O standard based simulation is implemented Xilinx software in order to design energy efficient VCM (Visitor Counting Machine) on FPGA. SSTL stands for Stub Series Terminated Logic and FPGA means Field-programmable Gate Array. Kintex-7 is used to implement this design. We have analyzed the energy dissipation at different frequencies like 5 GHz, 25 GHz, 125 GHz, 625 GHz and 1 THz and observed that at 5GHz frequency, SSTL12 IOs standard dissipate less energy than all other available SSTL IO standards.

Keywords— Simulation, Energy Efficient, Bi-directional, VCM, I/O Standard, SSTL, FPGA.

I. INTRODUCTION

In order to reduce the overall energy dissipation of VCM (Visitor Counter Machine), we are using different types of IOs standards such as SSTL12, SSTL12_DCI, SSTL135, SSTL135_R with different frequencies, like 5GHz, 25GHz, 125GHz, 625GHz, 1THz. SSTL means Stub Series Terminated Logic, is group of electrical standards for driving in transmission line, which is used in DRAM (Dynamic Random-Access Memory) based DDR (Double-Data-Rate) memory IC's. SSTL12 means Stub Series Terminated Logic, which can operate in 1.2 V. SSTL12_DCI means Stub Series Terminated Logic, which can operate in 1.2 V and DCI is versions only available for unidirectional (input or output) signals. SSTL135 means Stub Series Terminated Logic, which can operate in 1.35 V. SSTL135_R means Stub Series Terminated Logic, which can operate in 1.35 V, and R means reduced drive-strength R standards versions of the standard drivers, which preferred for short, point-point board topologies.

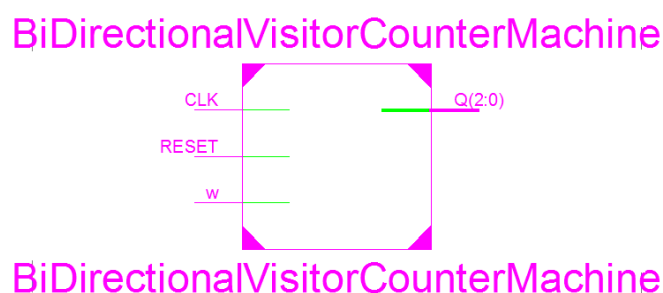


Fig. 1. Block diagram of VCM (Visitor Counter Machine).

Here VCM will give 3 bits output which is Q_0 , Q_1 and Q_2 . Bi-directional VCM have three inputs: one is CLK means clock input, another is RESET input which will give the opportunity to reset the program and last input is w, which will connect with the sensor device like Infrared sensors (IR) sensor. That means depending on the changes of IR sensors values it will count the visitor. Starting from 0, VCM can count 7 entities and after that it will reset and start from 0.

II. LITERATURE REVIEW

In previous we have implemented Bi-directional Visitor Counting Machine in PIC16F887 Microcontroller in our South Asian University, New Delhi, India. We have used IR sensor, IR receiver, and JHD 162A LCD display. That was implemented in Hardware Simulation Lab. We have written code in C by using MPLAB software. We have completed that project in Embedded System Course. Now we have implemented in Xilinx software and analysis the energy for that project.



Fig. 2. Functional block diagram of VCM Machine by PIC 16F887 Microcontroller.

In figure 2, we have given the functional block diagram of VCM machine by using PIC16F887 microcontroller. Here, IR Transmitter means Infra Red transmitter will transmit infra red ray and receiver will receive the infra red, whenever visitor will cross over in between of IR transmitter and detector that means there will be any interruption. That means there will voltage change. This interruption signal will give it to the microcontroller. Any microcontroller will count the number of visitors will give the output to the LCD display. For Microcontroller PIC 16F887, we have used MPLAB software, and we wrote code in C. Here that project's most difficult part was that how much the distance it will take in between of IR Transmitter and Receiver, whenever we got that then it solve very easily. Another difficult part was that how much time do we need to make to reset the LCD's output value?

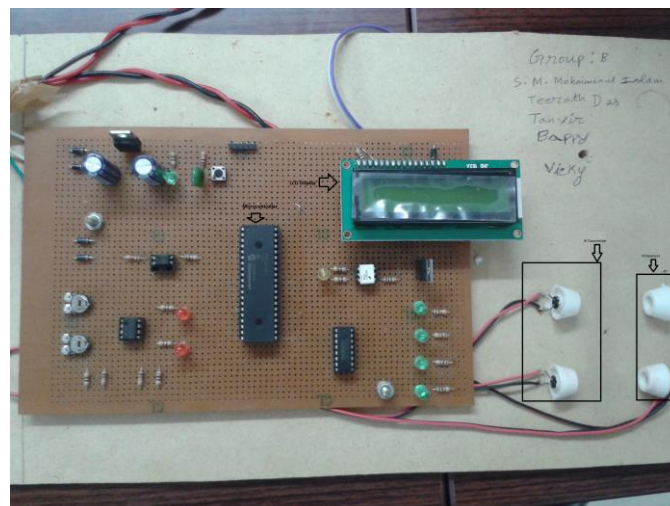


Fig. 3. Prototype of VCM by PIC 16F887 Microcontroller.

In Figure 3, we have showed the prototype of VCM (Visitor Counting Machine) by PIC 16F887 Microcontroller. Power is proportionally related to frequency. If frequency is increasing, there will be increase in power consumption irrespective of IO standard and also if frequency is decreasing, there will be decrease in power consumption [1]. SSTL standard buffers are general purpose IOs. In our practical life like in Indian Metro Railway station it can also implement. Now a day, the hot discussion of FPGA or microcontroller, which one should to use for any project. FPGAs are going to rule in research field because of their flexibility, better power efficiency and decreasing prices [2]. IR (Infrared) sensor is a device which is able to emit and/or able to detects the infrared radiation. IR sensors can measure the heat of an object or detect motion [3]. Many kinds of sensors are available in market one of them is PIR. PIR means passive infrared sensor. PIR is an electronic sensor which can measure IR light radiating from in its field [4]. PIR-sensor able to consume the power [5] and its application is in motion detection, ultra sonic signal coding [6], and wireless networks [7]. Most applications for the monitoring of human activities in an environment are based on video sensor data [8].

III. POWER CALCULATIONS

A. Calculations for SSTL12 I/O STD

TABLE I. TABLE FOR SSTL12 I/O STD.

	5 GHz	25 GHz	125GHz	625GHz	1THz
Clocks	0.022	0.109	0.543	2.714	4.342
Logic	0.001	0.002	0.008	0.036	0.057
Signals	0.003	0.015	0.077	0.386	0.617
IOs	0.040	0.140	0.640	3.138	5.012
Leakage	0.079	0.079	0.082	0.095	0.111
Total	0.145	0.345	1.350	6.369	10.139

In Table I, Selected IO standards is SSTL12, it's operating voltage is 1.2 V. Here we are taking 5 different device operating frequencies that start from 5 GHz and end with 1 THz. Intermediate frequencies are 25GHz, 125GHz and 625GHz. When we scale down from 1 THz to 5GHz, there is 99.49%, 98.24%, 99.51%, 99.20%, 28.82%, 98.57% reduction in clock energy, logic energy, signal energy, IOs energy and leakage energy respectively.

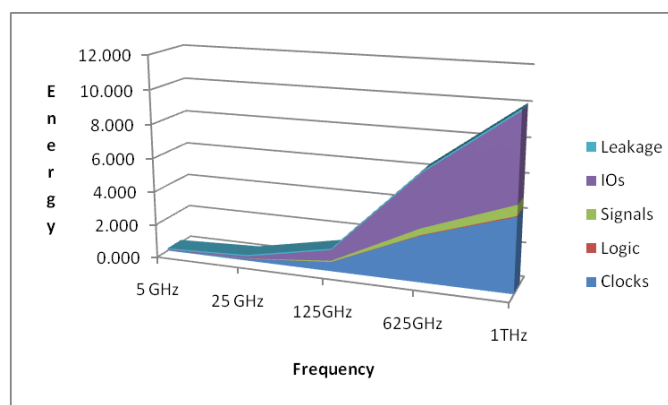


Fig. 4. Energy vs Frequency curve for SSTL12 I/O STD.

In Figure 4, leakage energy, IOs energy, signals energy, logic energy and clocks energy is represented using light blue color, purple color, olive green color, dark red color and blue color and its magnitude are 0.145J, 0.345J, 1.350J, 6.369J and 10.139J. These energy are the lowest at 5 GHz and highest at 1 THz.

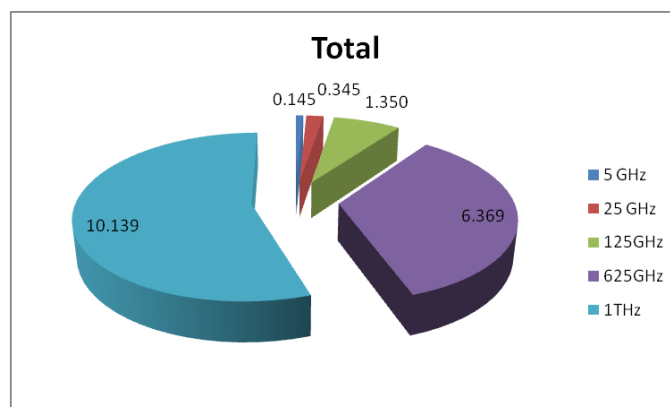


Fig. 5. Total energy dissipation different frequency for SSTL12 I/O STD.

In Figure 5, total energy on 5GHz, 25GHz, 125GHz, 625GHz and 1THz. We are representing using blue color, red color, olive green color, purple color and light blue color. This consumption is the lowest at 5 GHz and highest at 1 THz.

B. Calculations for SSTL12_DCI I/O STD

TABLE II. TABLE FOR SSTL12_DCI

	5 GHz	25 GHz	125GHz	625GHz	1THz
Clocks	0.022	0.109	0.543	2.714	4.342
Logic	0.001	0.002	0.008	0.036	0.056
Signals	0.003	0.015	0.076	0.380	0.609
IOs	0.079	0.179	0.679	3.178	5.052
Leakage	0.079	0.080	0.082	0.096	0.111
Total	0.184	0.385	1.388	6.404	10.170

In Table II, Selected IO standards is SSTL12_DCI, its operating voltage is 1.2 V and DCI is versions only available for unidirectional (input or output) signals. Here we are taking 5 different device operating frequencies that start from 5 GHz and end with 1 THz. Intermediate frequencies are 25GHz, 125GHz and 625GHz. When we scale down from 1 THz to 5GHz, there is 99.49%, 98.21%, 99.51%, 98.44%, 28.83%, 98.19% reduction in clock energy, logic energy, signal energy, IOs energy and leakage energy respectively.

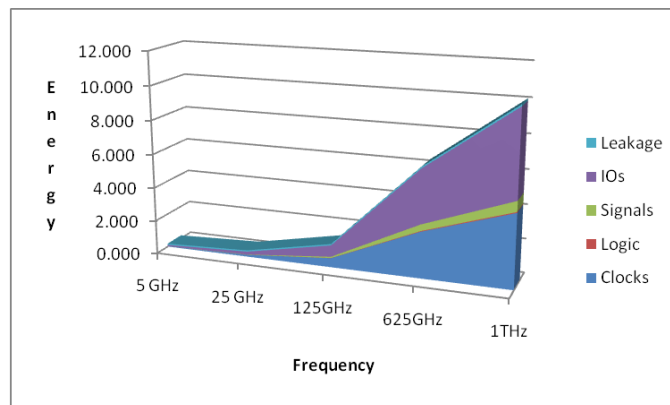


Fig. 6. Energy vs Frequency curve for SSTL12_DCI I/O STD.

In Figure 6, leakage energy, IOs energy, signals energy, logic energy and clocks energy is represented using light blue color, purple color, olive green color, dark red color and blue color and its magnitude are 0.184J, 0.385J, 1.388J, 6.404J and 10.170J. This energy is the lowest at 5 GHz and highest at 1 THz.

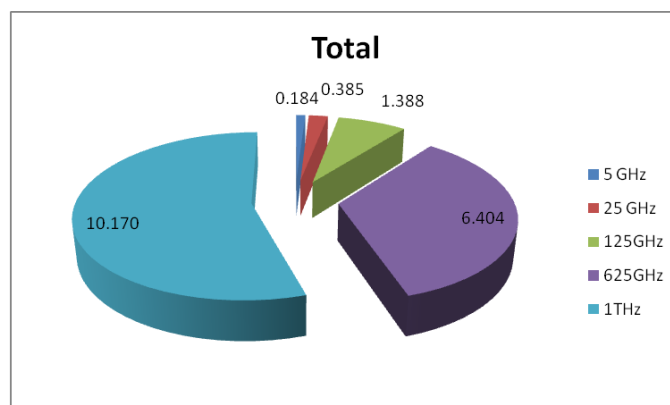


Fig. 7. Total energy dissipation different frequency for SSTL12_DCI I/O STD.

In Figure 7, total energy on 5GHz, 25GHz, 125GHz, 625GHz and 1THz. We are representing using blue color, red color, olive green color, purple color and light blue color. This consumption is the lowest at 5 GHz and highest at 1 THz.

C. Calculations for SSTL135 I/O STD

TABLE III. TABLE FOR SSTL135

	5 GHz	25 GHz	125GHz	625GHz	1THz
Clocks	0.025	0.127	0.637	3.183	5.093
Logic	0.001	0.002	0.008	0.036	0.058
Signals	0.002	0.011	0.056	0.282	0.452
IOs	0.080	0.355	1.728	8.597	13.748

Leakage	0.079	0.080	0.084	0.122	0.178
Total	0.187	0.575	2.513	12.220	19.529

In Table III, Selected IO standards is SSTL135, its operating voltage is 1.35 V. Here we are taking 5 different device operating frequencies that start from 5 GHz and end with 1 THz. Intermediate frequencies are 25GHz, 125GHz and 625GHz. When we scale down from 1 THz to 5GHz, there is 99.51%, 98.28%, 99.56%, 99.42%, 55.62%, 99.04% reduction in clock energy, logic energy, signal energy, IOs energy and leakage energy respectively.

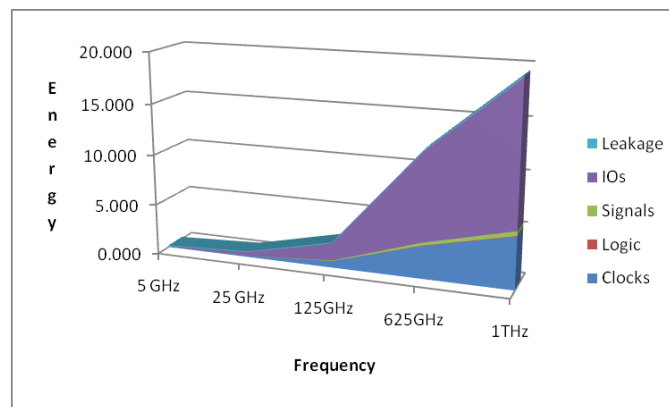


Fig. 8. Energy vs Frequency curve for SSTL135 I/O STD.

In Figure 8, leakage energy, IOs energy, signals energy, logic energy and clocks energy is represented using light blue color, purple color, olive green color, dark red color and blue color and its magnitude are 0.187J, 0.575J, 2.513J, 12.220J and 19.529J. This energy is the lowest at 5 GHz and highest at 1 THz.

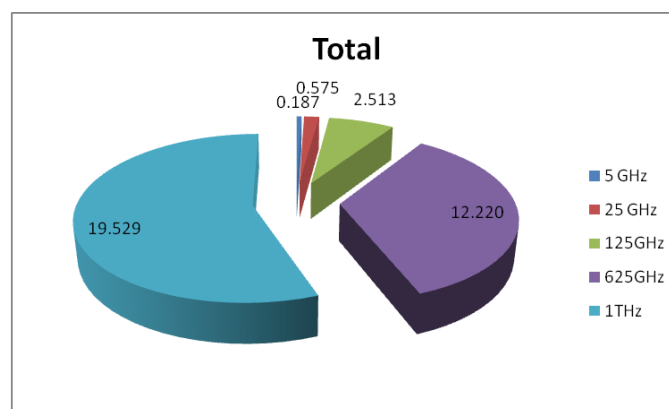


Fig. 9. Total energy dissipation different frequency for SSTL135 I/O STD.

In Figure 9, total energy on 5GHz, 25GHz, 125GHz, 625GHz and 1THz. We are representing using blue color, red color, olive green color, purple color and light blue color. This consumption is the lowest at 5 GHz and highest at 1 THz.

D. Calculations for SSTL135_R I/O STD

TABLE IV. TABLE FOR SSTL135_R

	5 GHz	25 GHz	125GHz	625GHz	1THz
Clocks	0.025	0.127	0.637	3.183	5.093
Logic	0.001	0.002	0.008	0.036	0.058
Signals	0.002	0.011	0.056	0.282	0.452
IOs	0.053	0.229	1.107	5.502	8.798
Leakage	0.079	0.080	0.083	0.106	0.136
Total	0.160	0.449	1.891	9.109	14.537

In Table IV, Selected IO standards is SSTL135_R, its operating voltage is 1.35 V and R means reduced drive-strength R standards versions of the standard drivers, which preferred for short, point-point board topologies. Here we are taking 5 different device operating frequencies that start from 5 GHz and end with 1 THz. Intermediate frequencies are 25GHz, 125GHz and 625GHz. When we scale down from 1 THz to 5GHz, there is 99.51%, 98.28%, 99.56%, 99.40%, 41.91%, 98.90% reduction in clock energy, logic energy, signal energy, IOs energy and leakage energy respectively.

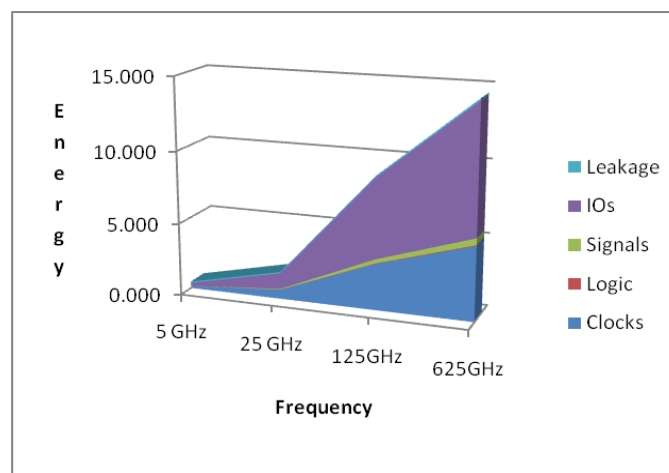


Fig. 10. Energy vs Frequency curve for SSTL135_R I/O STD.

In Figure 10, leakage energy, IOs energy, signals energy, logic energy and clocks energy is represented using light blue color, purple color, olive green color, dark red color and blue color and its magnitude are 0.160J, 0.449J, 1.891J, 9.109J and 14.537J. This energy is the lowest at 5 GHz and highest at 1 THz.

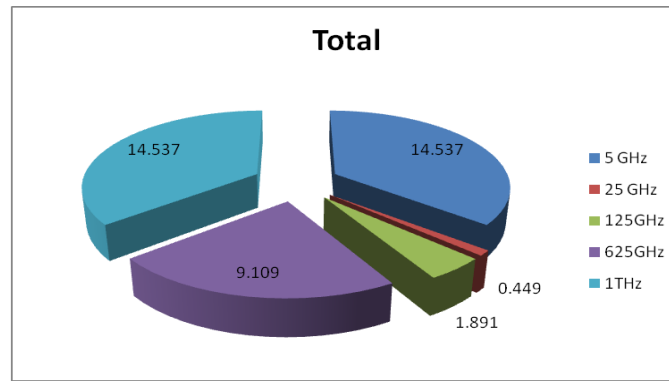


Fig. 11. Total energy dissipation different frequency for SSTL135_R I/O STD.

In Figure 11, total energy on 5GHz, 25GHz, 125GHz, 625GHz and 1THz. We are representing using blue color, red color, olive green color, purple color and aqua color. This consumption is the lowest at 25 GHz.

E. Comparing with SSTL12 and SSTL12_DCI I/O STD

TABLE V. TABLE FOR COMPARING WITH SSTL12 AND SSTL12_DCI IOS WITH SIGNALS, LOGIC AND CLOCK ENERGIES

		Clocks	Logic	Signals
5 GHz	<i>SSTL12</i>	0.022	0.001	0.003
	<i>SSTL12_DCI</i>	0.022	0.001	0.003
25 GHz	<i>SSTL12</i>	0.109	0.002	0.015
	<i>SSTL12_DCI</i>	0.109	0.002	0.015
125 GHz	<i>SSTL12</i>	0.543	0.008	0.077
	<i>SSTL12_DCI</i>	0.543	0.008	0.076
625 GHz	<i>SSTL12</i>	2.714	0.036	0.386
	<i>SSTL12_DCI</i>	2.714	0.036	0.380
1 THz	<i>SSTL12</i>	4.342	0.057	0.617
	<i>SSTL12_DCI</i>	4.342	0.056	0.609

In Table V, we have compared with SSTL12 and SSTL12_DCI IOs standard with each sample frequencies such that 5GHz, 25GHz, 125GHz, 625 GHz. In this table we have taken for Signals, Logic and Clock energies value. In this table we can take decision easily that theirs value are almost same.

TABLE VI. TABLE FOR COMPARING WITH SSTL135 AND SSTL135_R IOS WITH SIGNALS, LOGIC AND CLOCK ENERGIES

		Clocks	Logic	Signals
5 GHz	<i>SSTL135</i>	0.025	0.001	0.002

	<i>SSTL135_R</i>	0.025	0.001	0.002
25 GHz	<i>SSTL135</i>	0.127	0.002	0.011
	<i>SSTL135_R</i>	0.127	0.002	0.011
125 GHz	<i>SSTL135</i>	0.637	0.008	0.056
	<i>SSTL135_R</i>	0.637	0.008	0.056
625 GHz	<i>SSTL135</i>	3.183	0.036	0.282
	<i>SSTL135_R</i>	3.183	0.036	0.282
1 THz	<i>SSTL135</i>	5.093	0.058	0.452
	<i>SSTL135_R</i>	5.093	0.058	0.452

In Table VI, we have compared with SSTL135 and SSTL135_R IOs standard with each sample frequencies such that 5GHz, 25GHz, 125GHz, 625 GHz. In this table we have taken for Signals, Logic and Clock energies value. In this table we can take decision easily that theirs value are almost same.

Last of all we left only IOs energy for different IOs standard and previous graph we have seen that only 5 GHz dissipate less energy. Here we will not consider leakage energy.

F. Comparing with different I/O STD at 5 GHz frequency for IOs energy

TABLE VII. TABLE FOR DIFFERENT IOs AT 5 GHZ FREQUENCY

	SSTL12	SSTL135_R	SSTL12_DCI	SSTL135
IOs	0.040	0.053	0.079	0.080

In Table VII, we have showed the different IOs standard at 5 GHz frequency IOs energy value. Here, for SSTL12, SSTL135_R, SSTL12_DCI and SSTL135 dissipate energy for IOs according to 0.040J, 0.053J, 0.079J and 0.080J.

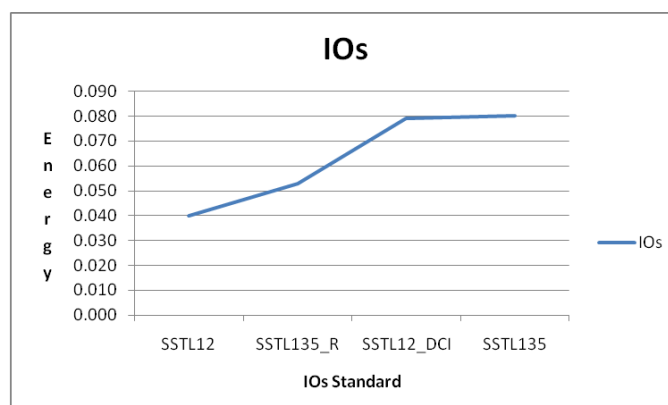


Fig. 12. Total energy dissipation at 5GHZ frequency for SSTL IOs Standard.

For Figure 12, total energy dissipation at 5 GHz frequency for different SSTL IOs standard curve has given. In this curve, energy dissipation of SSTL12 IOs Standard is much lesser than others. And again we have seen that this curve SSTL135_R is dissipating higher energy than SSTL12 but from SSTL12_DCI to SSTL 135 increase

very less comparison with SSTL12 and SSTL135_R. Finally, we can easily conclude that only SSTL12 for this VCM at 5GHz frequency dissipate less energy.

IV. CONCLUSIONS

We have tried to find out the less energy dissipation for different SSTL IOs STD which is implemented on Kintex-7 FPGA. We have done only simulation in Xilinx ISE 14.6 software and found that there is 24.52%, 49.36% and 50% the less energy dissipate for will SSTL12 IOs standard at 5GHz frequency as compared to SSTL135_R, SSTL12_DCI and SSTL135 respectively.

V. FUTURE SCOPE

We have implemented this design on 28nm FPGA, there is open scope to redesign this MBCCS on next generation FPGA and even lower 7nm future FPGA. Here, we have used different IOs standards like SSTL12, SSTL12_DCI, SSTL135, SSTL135_R, there is open scope to use other energy efficient IO Standards for making this design low power.

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