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Effect of Frequency on Energy Efficient Transceiver Design

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***Abstract*— We have observed the different chip power which are clustered on UART device, example IOs, leakage and total power. This through experiment is done at a frequency of 1 GHz, having a duty cycle of 50% and 1ns time period. We did our experiment with Virtex 4, Virtex 5, Virtex 6, Spartan3 and Spartan 6 FPGA. In the experiment we found Spartan 6 uses the least amount of power among all the FPGA used in the experiment.**
Keywords— FPGA, Power, Voltage, UART, Frequency.

1. Introduction

World is more relying on coal and natural resources for the generation and supply of electricity and this is possibly disturbing the global climate. Not only the world's population is rapidly increasing but the industrialization is also happening [1]. So to fulfil the everyone's need of energy is quiet difficult [2]. In order to minimize the energy consumption in communication network we have designed UART using different nanometers FPGA, which consumes least amount of energy. UART stands for Universal Asynchronous Receiver Transmitter. UART is running at a frequency of 1 GHZ, duty cycleof 50% and 1 ns time period. Duty cycle is the time period for which the signal is used. From the power and duty cycle relation = (PW/T)∗100, where D is duty cycle, PW is pulsewidth T is the time period of the signal. Data in UART is transmitted at a specific frequency known as Baudrate [3]. The time procedure involved in UART is shown in figure 1 the data is sampled when the baud rate of receiever and transmitter matches perfectly.

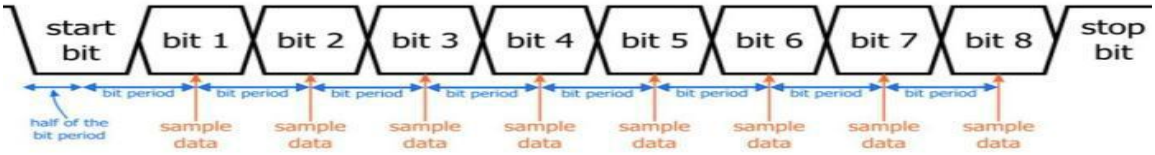

Figure 1. Data transfer in UART

2. Related Work

T.Taun ET. al. [4] a low power 90nm FPGA is designed by the authors, which is used for the application of battery powered devices. B. Pandey ET. al. [5] authors designed

a system using Virtex-6 FPGA, which checks the reduction of leakage power with different IO standards. In this design dynamic voltage scaling is also done in Vedic multiplier. B. Pandey ET. al. [6] energy efficient Gurumukhi Unicode Reader (GUR) is designed by the authors on FPGAs, which is done at a frequency 0f 1GHz by varying IO standards. Md. H. Rais ET. al. [7] with the help of Virtex-5 FPGA authors have designed an efficient hardware for advanced encryption of cryptographic algorithm. K. Rrcan ET. al. [8] low energy high performance hardware is demonstrated by the researchers, which is used for high efficiency video encoding using Virtex-6 FPGA. But in our research we have designed an energy efficient transceiver using different nanometer technology FPGA which is operated at 1GHz frequency.

3. Experimental Section

The experiment we performed is done on XILINX 14.1 ISE design. The different FPGA used are Virtex-4, Virtex 5, Virtex-6, Spartan-3, and Spartan 6. The code of UART is written in Verilog Hardware Description Language. We have tested UART power on X power Analyzer tool in XILINX simulator at 1 GHZ frequency, having 1 ns time period.

4. Explanation

The power table of Virtex-4, Virtex-5 and Virtex-6 FPGA is shown in table1.

Table 1. Supply power of Virtex 4, Virtex 5 and Virtex 6 FPGA

Supply Power	Virtex 4	Virtex 5	Virtex 6
IOs	0.011	0.014	0.017
Leakage	0.167	0.321	0.027
Total	0.204	0.350	0.063

The power table of Spartan- 3 and Spartan- 6 is shown in table2.

Table 2. Supply power of Spartan 3 and Spartan 6 FPGA

Supply Power	Spartan 3	Spartan 6
IOs	0.017	0.025
Leakage	0.027	0.014
Total	0.063	0.055

5. POWER ANALYSIS

A. Power Analysis of Virtex 4 v/s Virtex 5 v/s Virtex 6

At 1 GHz frequency Virtex 4 consumes least amount of IOs power. But for leakage power and total power Virtex6 is power efficient. The power comparison shown in figure 2.

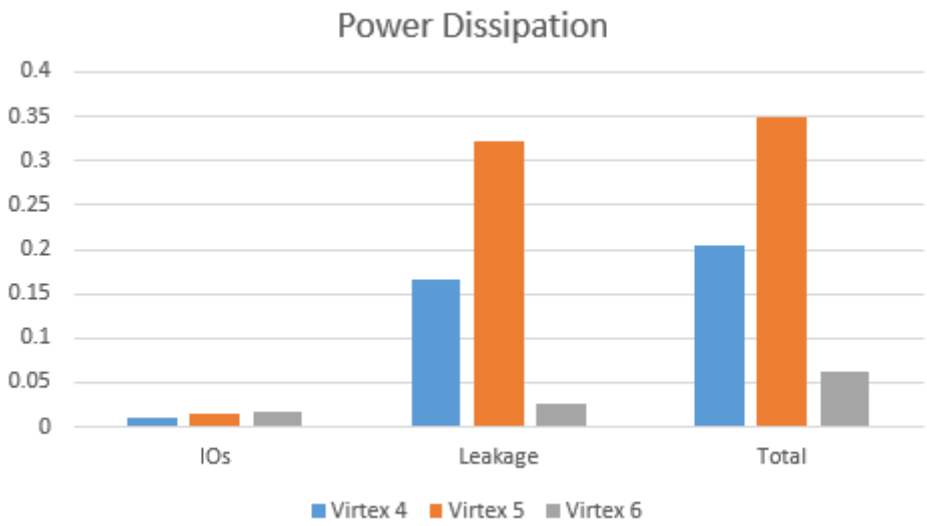

Figure 2. Power Analysis of Virtex-4 v/s Virtex-5 v/s Virtex-6

B. Power Analysis of Spartan 3 and Spartan 6

When frequency is 1 GHz Spartan-6 consumes least amount of leakage and total power in comparison to Spartan-3 and for IOs power Spartan-3 requires least amount of power. The different power comparison is shown in Figure 3.

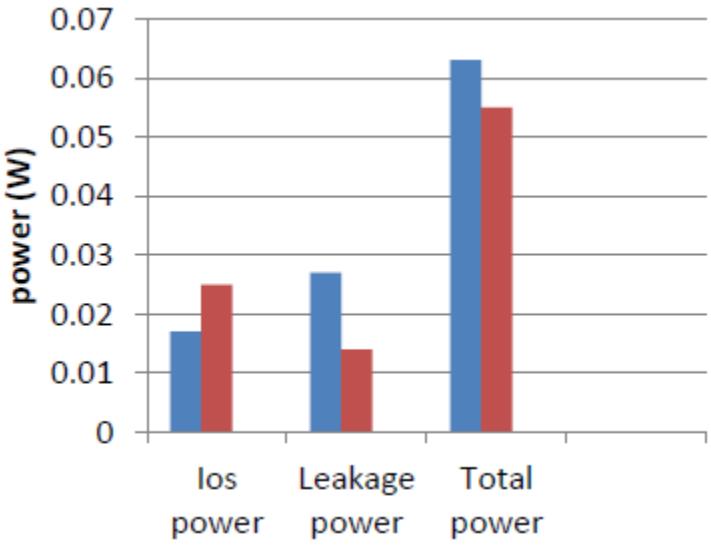

Figure 3. Power Analysis of Spartan-3 (Blue Color) and Spartan-6 (Red Color)

C. Power Analysis of Virtex 4 v/s Virtex 5 v/s Virtex 6 v/s Spartan 3 and Spartan 6.

When we compare all the FPGA at 1 GHZ frequency we found that Spartan 6 FPGA consumes the least amount of leakage power and total power but for IOs power Virtex 4 is most power efficient.S

6. Results

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It is observed that at 1GHz frequency Spartan 6 FPGA is most power efficient for leakage and total power. The percentage variation in leakage power and total power with Virtex 4, Virtex5, Virtex 6 and Spartan 3 is as 91.61%, 95.638%, 48.148%, 48.148 and 73.039%, 84.285%, 12.698%,12.698% respectively. For IOs power Virtex 4 is power efficient, Virtex 4 consumes 21.42% less power than Virtex 5, 54.54% less power than Virtex 6, 54.54% less power than Spartan 3 and 56% less power than Spartan 6.

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7. Conclusion

We are comparing the power utilization of Spartan-3 and Spartan-6 FPGA by increasing the voltage of UART, we found that in case of IOs power Spartan-3 FPGA is more power efficient than Spartan-6 FPGA. And for leakage and total power Spartan-6 FPGA should be used because it consumes less power than Spartan-3 FPGA. The power analysis of UART is done on Xilinx 14.1 ISE Design software and code of UART is written in Verilog module. After analyzing the results we can say that Spartan-6 FPGA is more reliable over Spartan-3 FPGA.

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