Gyancity Journal of Engineering and Technology,
Vol.3, No.1, pp. 17-22, January 2017
ISSN: 2456-0065 DOI: 10.21058/gjet.2017.31003

LVCMOS IO Standards Based Processor Specific Green Comparator Design

[1]Chandrashekhar Patel, [2]Parth Gautam, [3]Priyanka Mehra,[4]Ankita Pundir,[5]Shivani Sharma
[1,2,3,4,5] Dev Sanskriti Vishvavidyalaya Haridwar India
[1]shekharrockin1988@gmail.com,[2] parth.gautam@dsvv.ac.in,
[3]priyamehra1201@dsvv.ac.in,[4]ankitapundir777@gmail.com,[5]tanu.sharma177@gmail.com

Abstract

In this research paper we have designed green comparator to attain less power consumption. We have implemented our design with LVCMOS IOs standard which is stands for Low voltage complementary Metal Oxide Semiconductor. We have taken different frequency range (1GHz, 2GHz, 3GHz) at which we have tested the power consumption by the different LVCMOS IO standards. When we migrate from LVCMOS25 to LVCMOS12 at 1GHz then we got 4.22% of power reduction. At 2GHz when we migrate from LVCMOS25 to LVCMOS12 then we got 11.08% of power reduction. At 3GHz when we migrate from LVCMOS25 to LVCMOS12 then we got 15.026% of power reduction. We have designed our comparator on 28nm Aritx-7 FPGA family.

Keywords: LVCMOS IO standard, Low Power, Energy Efficient, 28 nm FPGA, Comparator

1. Introduction

Comparators are the circuits which are crucial for compare two bit stream. The operations performed are (=,/=,<,>,<=,>=).Two inputs are taken and comparator perform the operation and gives the output either 'true or 'false'. In this paper we use two 8- bit input stream and 3-bit selection line to decide the operation. In the table1 the number of operations is performed by comparator are given.

Table1: Number of Operations

SEL	Operation
000	Equal to
001	Not Equal to
010	Greater Than
011	Less Than

Gyancity Journal of Engineering and Technology,
Vol.3, No.1, pp. 17-22, January 2017
ISSN: 2456-0065 DOI: 10.21058/gjet.2017.31003

101	Greater than or equal
111	Less than or equal

1.1. Low Voltage Complementary MOS (LVCMOS)

We have design our green comparator which is based on LVCMOS IO standards. LVCMOS is stands for Low Voltage Complementary Metal Oxide Semiconductor. In this paper we have worked with four types of LVCMOS classified as LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12.Unidirectional and bidirectional techniques of LVCMOS is shown in figure 1 and figure 2

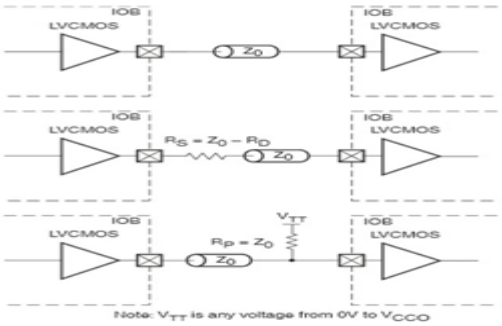

Fig. 1: Unidirectional Termination of LVCMOS IO Standard [5]

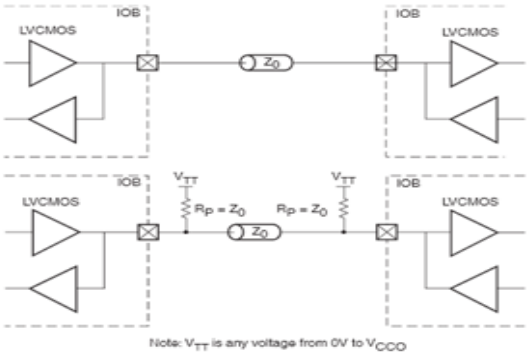

Fig. 2: Bidirectional Termination of LVCMOS IO Standard [5]

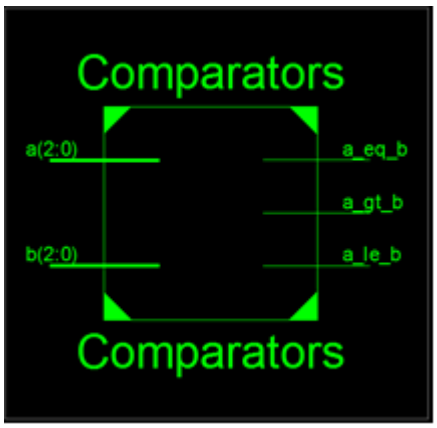

Fig. 3: Top Level of Schematic of Comparator

Gyancity Journal of Engineering and Technology,
Vol.3, No.1, pp. 17-22, January 2017
ISSN: 2456-0065 DOI: 10.21058/gjet.2017.31003

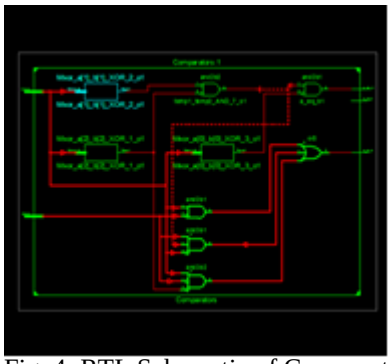

Fig. 4: RTL Schematic of Comparator

In figure 3 and figure 4 we have shown the Top Level of Schematic of Comparator and RTL Schematic of Comparator.

2. Related Work

In our research, we come across with many direct applications of LVCMOS in energy efficient design like power optimized optical transmitter [1], low power ROM [2]. We observed a research gap that LVCMOS was never used in energy efficient green comparator design. In this work, we are trying to fill this research gap with design of green comparator on 40nm FPGA. The main motivation behind development of comparator comes after study of implementation of various arithmetic circuits on FPGA. “Ekadhiken purven” is a Vedic mathematics based formula used to calculate square [3], energy efficient design and implementation of ALU [4], Green ECG Machine [5]. IO standards were also used in energy efficient design of 28nm FPGA [6]. There are many low power techniques. Those are widely used in practice for design of digital system [7]. Power consumption analysis of BCD adder [8] in this work. HSTL IO Standards Based Processor Specific Green Counter [9]. Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling in Vedic Multiplier on Virtex-6 FPGA [10].

3. Results

We have designed our comparator through VHDL language and implemented it on 28nm FPGA AIRTX-7 family. For the power analysis we used the Xpower analyzer tool in Xilnix software

Table 1: Power Consumption at 1GHz

	Dynamic	Quiescent	Total
LVCMOS12	0.0085	1.749	1.834
LVCMOS15	0.103	1.750	1.853
LVCMOS18	0.119	1.751	1.870
LVCMOS25	0.162	1.753	1.915

Gyancity Journal of Engineering and Technology,
Vol.3, No.1, pp. 17-22, January 2017
ISSN: 2456-0065 DOI: 10.21058/gjet.2017.31003

In table 1, we try to calculate total power consumption at 1GHz. Here when we migrate from LVCMOS25 to LVCMOS12 then we reduce the 4.22% in total power consumption. We also shown this analysis by the bar graph as shown in Fig. 5

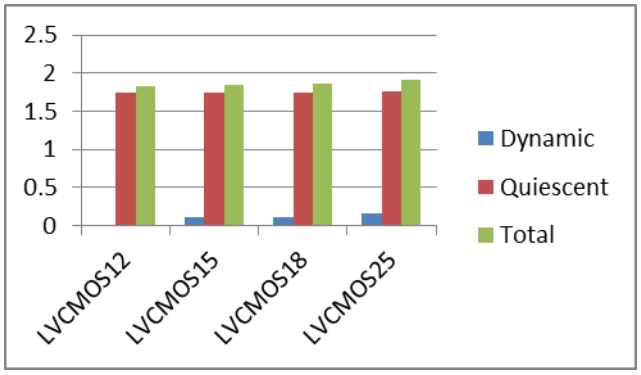

Figure 5: Power analysis at 1GHz

Table 2: Power Consumption at 2GHz

	Dynamic	Quiescent	Total
LVCMOS12	0.204	1.754	1.958
LVCMOS15	0.258	1.756	2.014
LVCMOS18	0.307	1.758	2.066
LVCMOS25	0.437	1.764	2.202

In table 2, we try to calculate total power consumption at 2GHz. Here when we migrate from LVCMOS25 to LVCMOS12 then we reduce the 11.08% in total power consumption. We also shown this analysis by the bar graph as shown in Fig. 6

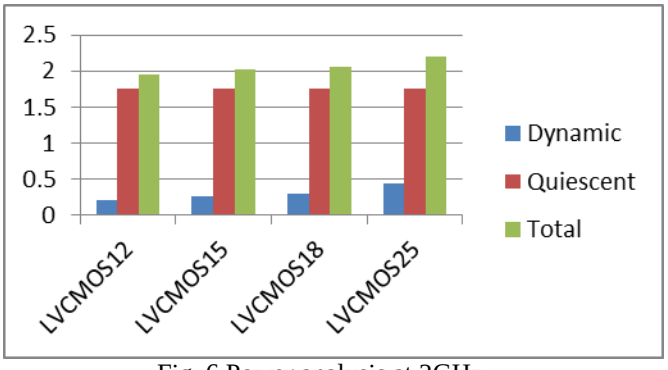

Fig. 6 Power analysis at 2GHz

Table 3: Power Consumption at 3GHz

	Dynamic	Quiescent	Total
LVCMOS12	0.306	1.758	2.064
LVCMOS15	0.387	1.761	2.149
LVCMOS18	0.461	1.765	2.226
LVCMOS25	0.656	1.773	2.429

ISSN: 2456-0065 DOI: 10.21058/gjet.2017.31003

In table 3, we calculate our total power consumption at 3GHz.Here when we switched from LVCMOS25 to LVCMOS12 then we reduce the 15.026% power consumption. We have also use the bar graph to show this analysis as shown in the figure7.

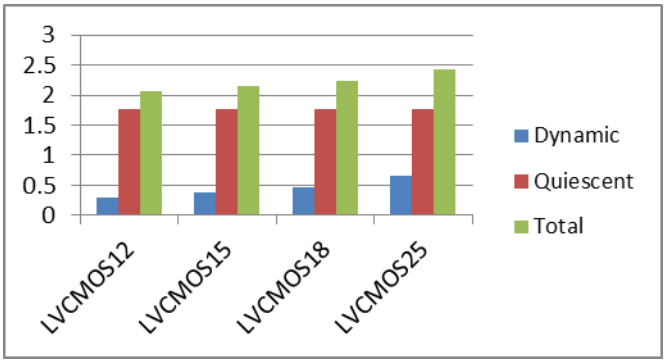

Fig. 7 Power analysis at 3GHz

4. Conclusion

In this work we have worked with three different frequency range and calculated total power consumption of comparator. We found that at 1 GHz when we migrate from LVCMOS25 to LVCMOS12 we reduce the power consumption by 4.22%. At 2GHz when we migrate from LVCMOS25 to LVCMOS12 we reduce the power consumption by 11.08%.At last when we switched from LVCMOS25 to LVCMOS12 we reduce the power consumption by 15.026%.

5. Future Scope

In this work, Comparator Design is implemented on 28nm on Airtex-7, but we have a scope to redesign this Comparator on latest 65nm Virtex-5 and 40nm Virtex-6, 90nm Virtex-4 FPGA to make the most energy efficient FIFO for processor. We can also take more frequency range to redesign energy efficient Comparator.

Acknowledgment

The author would like to acknowledge Gyancity Research Lab (India & Overseas) for their valuable support for the findings of this research paper.

References

[1] B. Das, A. Kiyani, V. Kumar, M.F.L. Abdullah, B. Pandey, "Power optimization of Pseudo Noise based optical transmitter using LVCMOS IO standard," in Power Generation System and Renewable Energy Technologies (PGSRET), 2015, pp.1-7, 10-11 June 2015

[2] L. Kalra, N. Bansal, R. Saini, M. Bansal, B. Pandey "LVCMOS I/O Standard Based Environment Friendly Low Power ROM Design on FPGA", IEEE International Conference on "Computing for Sustainable Global Development (INDIACOM), Bharati Vidyapeeth, Delhi, 11-13 March 2015.

[3] G. Verma, S. Maheshwari, S. K. Virdi, N. Baishander, I. Singh, B. Pandey, "Low Power Based Energy Efficient Squarer Design Using Ekadhikena Purvena on 28nm FPGA", International Conference on Recent trends on Computer Science and Electronics Engineering (RTCSE'16), 02-03 January, 2016, Kuala Lumpur, Malaysia.

[4] B. Pandey, J. Yadav, Y. Singh, R. Kumar, S. Patel, "Energy Efficient Design and Implementation of ALU on 40-nm FPGA", IEEE International Conference on Energy Efficient Technologies for Sustainability-(ICEETs), Kanyakumari, India, pp.45-50, April 2013

[5] S. Aggarwal, G. Verma, A. Kaur, B. Pandey, S. Singh and R. Kumar, "Green ECG Machine Design Using Different Logic Families", IEEE International Conference on Communication Systems and Network Technologies (CSNT), Gwalior, India, April 2015.

[6] B. Pandey, J. Yadav, M. Pattanaik "IO Standard Based Energy Efficient ALU Design and Implementation on 28nm FPGA", 10th IEEE India Conference (INDICON) 2013, IIT Bombay, India, December 2013

[7] G. Verma, M. Kumar, and V. Khare. "Low Power Techniques for Digital System Design." Indian Journal of Science and Technology 8, no. 17 (2015): 1.

[8] G. Verma, et al. "Power Consumption Analysis of BCD Adder using XPower Analyzer on VIRTEX FPGA." Indian Journal of Science and Technology.

[9] A.Saxena, A.Bhatt B.Pandey, P.Tripathi "HSTL IO Standards Based Processor Specific Green Counter." In International Journal of Control and Automation, Vol. 9, No. 7, (2016), pp. 331-342.

[10] B.Pandey, Md. Rahman, A.Saxena, A.Hussain, B.Das "Leakage Power Reduction with Various IO Standards and Dynamic Voltage Scaling in Vedic Multiplier on Virtex-6 FPGA". In Indian Journal of Science and Technology, Vol 9(25), July 2016.