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# Power and Time Delay Analysis of Simple Comparator Implemented On Different Type of FPGA

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***Abstract***

*In this particular work, we have implemented the algorithm of comparator on different version of FPGA like virtex-4, virtex-5, virtex-6, virtex-6(low power) and virtex-7. Using high performance Xilinx ISE software, we calculated the supply power and timing constraints like delay in timings from source pad to destination of the algorithm when implemented on different versions of FPGA.*

***Keywords: Low Power, FPGA, Time, High Performance, FPGA, delays***

## 1. Introduction

Technically, simple comparator compares two different values of voltage and current which is then analysed to check output of a digital signal results the larger value. Basically, it consists of high gain differential amplifiers. Electronic equipment encounters differential voltage in its system but it is compulsory for it to stay within the range specified by the manufacturer. The basic requirement is substantially lower than the power supply voltage that is released from the power stations. For the proper knowledge of this balancing of voltage, many type of parameters need to be considered like value of utilizied power at certain input-output standards and timing constraints such as delay. As it is observed that for different standards of inputs the rate of power consumed, varies. When this variation is notified then it becomes easier to configure whole system at the level of manufacturer specifications. A field programmable gate array is an integrated circuit which has wide variety of applications, it has a capability to program ROM chip. Different algorithm is applied on FPGA and experiment could be performed where xilinx ISE is the software that provides a facility of observing the various conditions virtually. Furthermore, power supply in electronic system are divided in four different categories like

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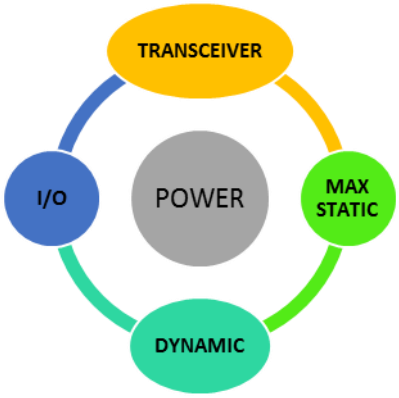


**Figure 1: The four different types of powers**

These type of power consumption gets reduced to its half when particular algorithm is implemented on FPGA. this programmable device ensures 71% lower power than other multi-chip solutions. FPGAs are the very cost effective and efficient. On the same side, every electronic device operates with a combination of power and timing. Basically, circuits supply power to interor parts of its system at certain time durations. The xilinx ISE software helps to analyse the duration gap i.e. delays taken by the algorithm of simple comparator with various values of inputs. Timing analysis has been done by implementing the algorithm on many versions of FPGA such as Virtex-4, Virtex-5, Virtex-6 and Virtex-6 low power.

## 2. Related Work

One of the researchers had done experiment with simple comparator to analyze the thermal property like measurement of very low response time to achieve minimum circuit complexity [1]. On the same side we had implemented the algorithm of simple comparator on multipurpose circuit board called FPGA to observe different values of power consumption. Whereas other authors has used simple comparator to analyze the dimensions of material with very small particle size by some sort of operation. Here we has experimented the utilization of power supply by simple comparator to operate certain operations [2]. Further, few researchers has used computer systems to detect the errors which results in the failure of operating system with the help of comparators coding. On the same side we had observed the conditions over which the simple comparator algorithm is compatible or not [3]. Moreover other scientist had performed experiment to use one of the input output standard to stimulate particular type of sensor. On the other side we had observed the different temperature conditions of the simple comparator code to which sensors with different specifications could be stimulated [4]. Other writers had mentioned all about the basic guidelines of input-output standards whereas we have implemented different input-output standards to have detailed knowledge of the algorithm [5]. In addition, FPGA was studied by some authors and they analyzed all about its packaging, placement and routing for any specific algorithm implemented on it. On the same side we had observed the occupancy of component by the simple comparator

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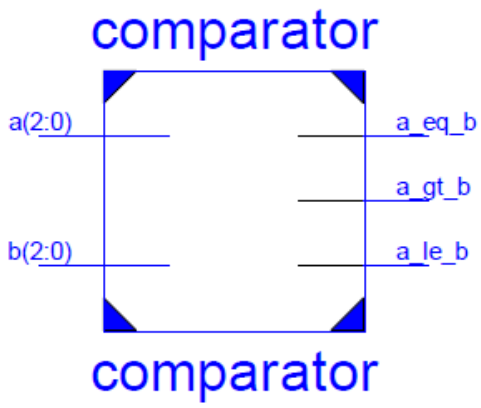
algorithm on the FPGA [6]. Furthermore, few researchers has implemented CORDC algorithm on FPGA and analyzed it whereas we studied all about the characteristics of simple comparator algorithm on various versions of FPGA. Timing analysis is another feature of electronics system that could help in calculating time related observation. Nowadays, most of the technical advancements are done on the basis of power utilization and its size. For this type of innovations, one must be aware about the fact that how much power is consumed by particular system. The same is done by some scientist, virtually using Xilinx, i.e. observing the timing constraint [8] and power [9] for different projects [11]. In contrary to this, we has compared level of power consumed and delays encountered by the simple comparator algorithm for different platforms of FPGA. Many experts have recorded timing constraints of the algorithm related to security system [10]; in this piece of work delay at output has been notified at various values of inputs.

## 3. Analysis

The code used for the study is an algorithm of a 2-bit magnitude comparator using logic gates such as XNOR, OR, AND, etc. the 3-bit magnitude comparator is a combinational circuit that compares two different numbers into three categories like less than, equal to and greater than. It is of two input and three indicator type of outputs.




(a) block diagram of the simple comparator

| Input | | Outputs | | |
|---|---|---|---|---|
| X | Y | X>Y | X=Y | X<Y |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |

(b) Truth Table

**Figure 2: diagram and table**

This code has been written in VDHL that is VHSIC hardware description language which is used in electronic for the automation digital designs. This type of programming is generally used for the parallel applications of various programs.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity comparator is
port( a,b : in unsigned(2 downto 0);  --3 bit numbers to be compared
        a_eq_b : out std_logic;  --a equals b
        a_le_b : out std_logic;  --a less than b
        a_gt_b : out std_logic   --a greater than b
      );
end comparator;

architecture gate_level of comparator is

signal temp1,temp2,temp3,temp4,temp5,temp6,temp7,temp8,temp9 : std_logic := '0';

BEGIN

temp1 <= not(a(2) xor b(2));  --XNOR gate with 2 inputs.
temp2 <= not(a(1) xor b(1));  --XNOR gate with 2 inputs.
temp3 <= not(a(0) xor b(0));  --XNOR gate with 2 inputs.
temp4 <= (not a(2)) and b(2);
temp5 <= (not a(1)) and b(1);
temp6 <= (not a(0)) and b(0);
temp7 <= a(2) and (not b(2));
temp8 <= a(1) and (not b(1));
temp9 <= a(0) and (not b(0));

a_eq_b <= temp1 and temp2 and temp3;  -- for a equals b.
a_le_b <= temp4 or (temp1 and temp5) or (temp1 and temp2 and temp6); --for a less
than b
a_gt_b <= temp7 or (temp1 and temp8) or (temp1 and temp2 and temp9); --for a greater
than b

end gate_level;
```

**Figure 3: VHDL code of simple comparator**

In the above code of two bit numbers are used for the comparison. There are nine different temporary variables used to store various type compares results. In the last four lines of the code three variable are defined which stores final result of two numbers that could be equal to, less than or greater than each other. It is very clear fact that whenever any algorithm is implemented on any type of integrated circuit, particular amount of power consumption take place such as I/O power, dynamic power, max static power and supply power. In this piece of work, we have done analysis on the amount of supply power utilized by the simple comparator algorithm when it was implemented on different categories of FPGAs like virtex-4, virtex-5, virtex-6, virtex-6 low power and virtex-7.

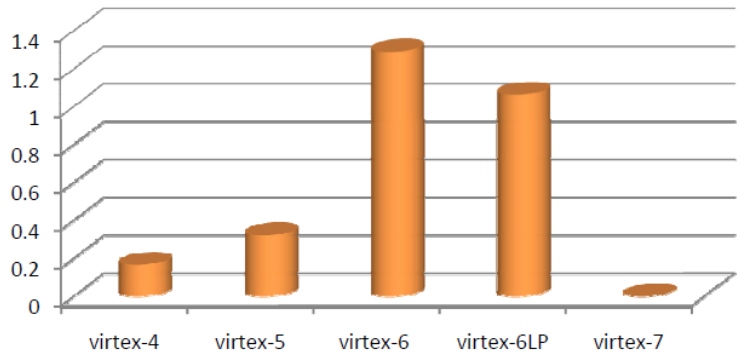



**Figure 4: graphical representation of supply power consumed**

Figure 4 represents the comparison between the powers consumed by different devices in the graphical form. From there it has been notified that the simple comparator was not able to become compactable with virtex-7. It is crystal clear

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from the graph that maximum supply power was consumed by virtex-6 and that of virtex-4 was least.

## 4. Timing Constraints

The following experiment was performed to observe the amount of delay encounted by the algorithm at encountered by the algorithm at three different destined places like a_eq_b, a_gt_b and a_le_b which are in short term presented in the upcoming graphs as eq, gt and le. To illustrate this a_eq_b stands for the output result represents that a is equal to b, a_gt_b refers to a is greater than b and a_le_b presents that a is less than b. the delay duration calculated in this findings is on the basis of three different input sources like 0,1 and 2. However, this observation involves four category of FPGA that is virtex-4, virtex-5, virtex-6 and virtex-6 low power as illustrated in upcoming paragraphs.

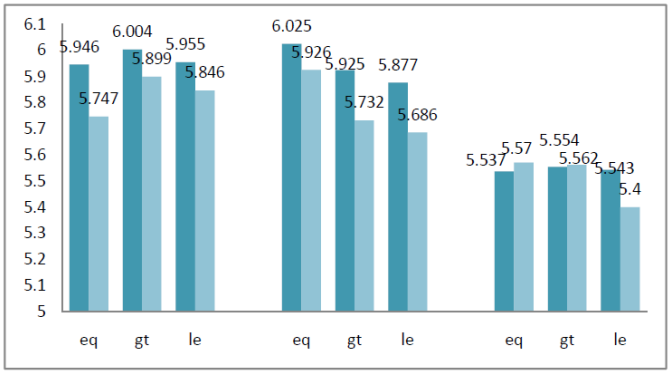


**Figure 5: Delay Analyzed at IO of schematic, implemented on VIRTEX-4 FPGA**

When the algorithm was implemented on virtex-4 FPGA, it has been observed that maximum delay time was calculated for a<1> and b<1> source pad. Further it shows declining pattern for delay time duration as shown in Figure 5.

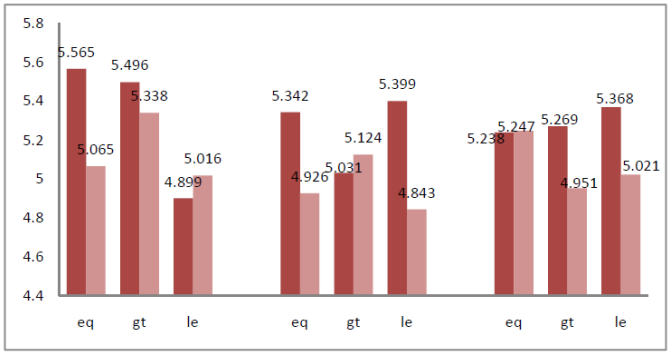


**Figure 6: Delay Analyzed at IO of schematic, implemented on VIRTEX-5 FPGA**

Figure 6, represent the data of delay time recorded for the algorithm of simple comparator which was implemented on virtex-5 version of FPGA. For instance,

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there is the overall fluctuating pattern observed at different outputs. Moreover, at the initial input, the delay time was at peak for the destined place of a_eq_b and that for the a_le_b is calculated to be least.

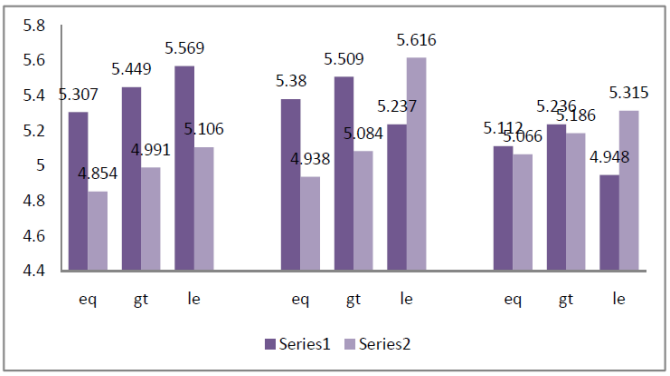


**Figure 7: Delay Analyzed at IO of schematic, implemented on VIRTEX-6 FPGA**

Figure 7, depicts information regarding the IO of schematic of simple comparator algorithm when implemented on virtex-6 type of FPGA. From where it is observed that the series one shows comparatively raised pattern than that of series two in the delay calculated. Therefore, only for b<1> source pad with destination path of a_le_b notified delay time is high.

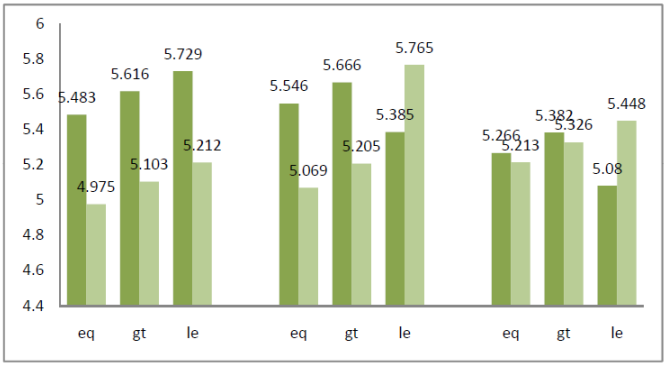


**Figure 8: Delay Analyzed at IO of schematic, implemented on VIRTEX-6 LOW POWER FPGA**

Figure 8, illustrates that among two source pad a and b, the delay measured is at peak. As the inputs goes from a<0> to a<2> and b<0> to b<2>, the value of delay gradually approaches nearly equal to the increasingly higher value.

## 5. Conclusion

Hammering the last nail, this experiment has been performed to analyze the power and timing constraints of the simple comparator algorithm with was implemented on different type FPGAs. It has been analyzed that the virtex-4 was notified to be the most efficient platform for the implementation of the algorithm. On the other hand, when the algorithm was processed on virtex-6 and

virtex-6 low power category of FPGA, there was a countable difference in between two type of source pad a and b, whereas in virtex-4 and virtex-5, there was very little variation in the time delay calculated.

## 6. Future Scope

This work of observation has a bright future scope as it is related to power as well as efficiency of particular system on FPGA. It is beneficial for the experiment like dealing with very high voltages and as simple comparator are the known for their property of differential amplification. So, this work could help in the initial steps of these types of experiments.

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