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Low Power Digital Clock Design Using LVCMOS Input/Output Standards on 45nm FPGA

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***Abstract*—How wonderful it would be if every device we use is energy efficient. This is an approach to design an efficient digital clock that consumes low amount of power. This is done by varying frequency to different levels and checking corresponding amount of energy consumed. Low Voltage Complementary metal oxide semiconductor i.e. LVCMOS and 45nm Spartan-6 FPGA family is used for simulation and amount of total power consumed is noted down. There is 90.02%, 98.88%, 99.86% and 100% reduction in the clock when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively.**

Keywords- Power, efficient, LVCMOS, Digital Clock, FPGA

1. Introduction

Digital Clock is a clock that displays the time digitally i.e.by digits or any symbols which is most commonly used electronic device. In order to have a look on its power consumption and efficiency we have tried to study upon different factors and finally on the total power dissipated at different frequencies. Results are noted down for family of Low Voltage Complementary Metal Oxide Semiconductor i.e. for LVCMOS12, LVCMOS15, LVCMOS18 and LVCMOS33.These are a low voltage class of complementary metal oxide semiconductor technology and have better performance as well as low power consumption.SPARTAN-6 family is used which has greatest system integration abilities to produce outcome. Some points about SPARTAN-6 are as follows:

- Has lowest total cost.
- The power consumed is almost half the power consumed by previous families.
- It offers more effective and efficient look up table i.e. LUT logic.
- Every CLB has two slices which are arranged side by side as a part of two vertical columns.
- Three Spartan-6 which are SLICEL, SLICEM and SLICEX.

2. Related Work

Spartan-6 FPGA, built on 45nm technology, is ideally suited for a range of advanced bridging applications found in automotive infotainment, consumer, and industrial automation [1]. This second section consists of the work which is somewhat different

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and is related to this work in some sort of senses. There are many papers which are already written relating to LVCMOS, FPGA [2-10]. Some of the paper that already done not exactly same work and have small similarities with this paper are as follows. GTL IO standards is used in Internet of Things Enable Processor Specific RAM Design on 65nm FPGA [6]. SSTL IO standards is used in Power Efficient Implementation of DES Security Algorithm on 28nm FPGA [7]. Pseudo Open Drain IO Standard is used to Energy Efficient Solar Charge Sensor Design on 20nm FPGA [8]. LVTTL IO standards is used to design Energy Efficient Watermark Generator Design and Implementation on FPGA [9] and LVDCI I/O Standard is used in Green Image ALU Design on Ultra Scale FPGA [10]. We are using LVCMOS IO standards in our work that is not covered by IO standard used in [6-10].

3. Analysis And Interpretation Of Power Dissipation In Digital Clock

Table 1: Values of Clock, Logic and Signal for LVCMOS12 & LVCMOS15

Frequency GHz	0.01	0.1	1	10	100
Clocks	0.000	0.002	0.016	0.143	1.434
Logic	0.000	0.000	0.002	0.016	0.040
Signals	0.000	0.000	0.005	0.053	0.522

There is 90.02%, 98.88%, 99.86% and 100% reduction in the clock when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 60%, 95%, 100% and 100% reduction in Logic when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 89.84%, 99.04%, 100% and 100% reduction in Signals when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively.

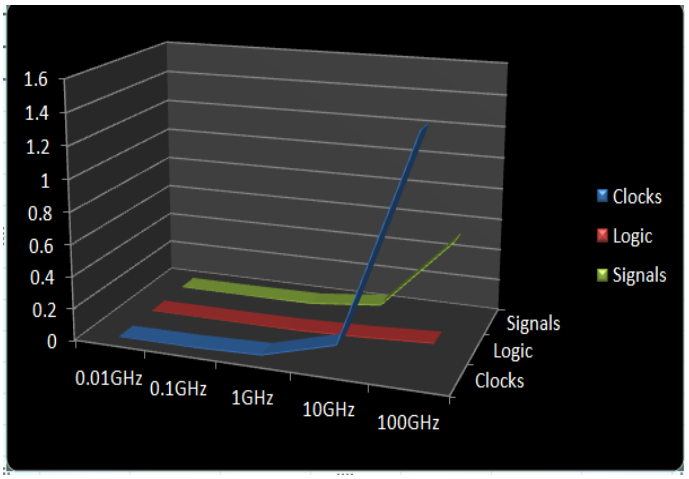

Figure1: Graph of Clock, Logic and Signals at different frequencies

Table 2: Values of I/Os, Leakage and Power at different Frequencies for LVCMOS12

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.001	0.009	0.090	0.948	9.480
Leakage	0.012	0.012	0.014	0.029	0.036
Total Power	0.014	0.0.24	0.127	1.190	11.511

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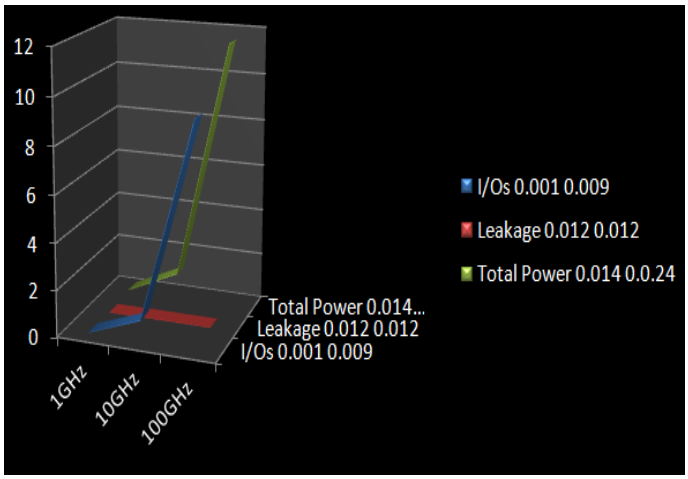

Figure 2: Graph of I/Os, Leakage and Power at different frequencies for LVCMOS12

There is 90%, 99.05%, 99.90% and 99.98% reduction in IOs when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 19.44%, 61.11%, 66.66% and 66.66% reduction in Leakage when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 89.66%, 98.89%, 99.79% and 99.87% reduction in Total Power when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively.

Table 3: Values of I/Os, Leakage and Power at different Frequencies for LVCMOS15

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.001	0.010	0.099	1.044	1.435
Leakage	0.013	0.013	0.014	0.032	0.036
Total Power	0.014	0.025	0.136	1.288	12.467

There is 90.16%, 99.05%, 99.90% and 99.99% reduction in IOs when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 11.11%, 61.11%, 63.88% and 63.88% reduction in Leakage when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 89.66%, 98.90%, 99.79% and 99.88% reduction in Total Power when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively.

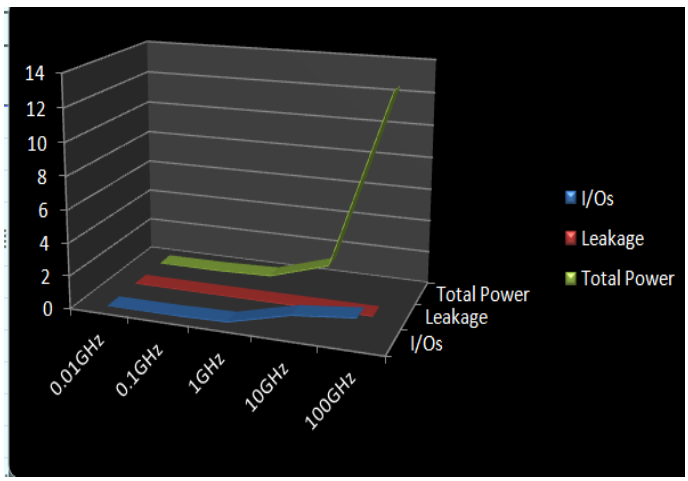

Figure3: Graph of I/Os, Leakage and Power at different frequencies for LVCMOS15

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Table 4: Values of Clock, Logic and Signal for LVCMOS18 & LVCMOS33

Frequency GHz	0.01	0.1	1	10	100
Clocks	0.000	0.002	0.017	0.160	1.597
Logic	0.000	0.000	0.002	0.016	0.039
Signals	0.000	0.001	0.006	0.061	0.592

There is 89.98%, 98.93%, 99.87% and 100% reduction in the clock when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 58.97%, 94.87%, 100% and 100% reduction in Logic when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 89.69%, 98.98%, 99.83% and 100% reduction in Signals when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively.

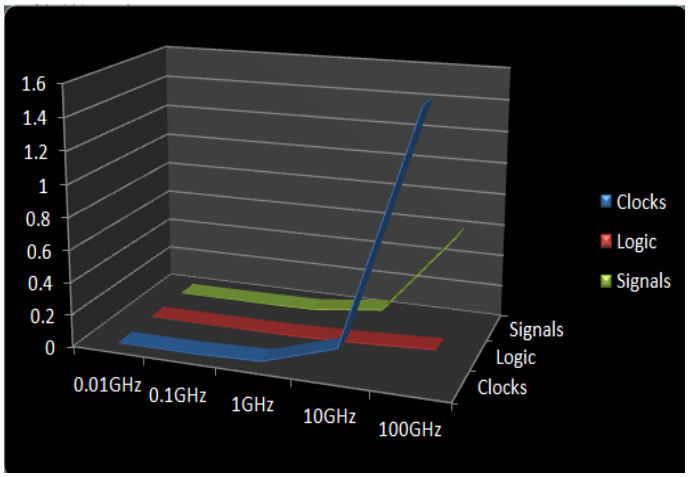

Figure4: Graph of Clock, Logic and Signals at different frequencies

Table 5: Values of I/Os, Leakage and Power at different Frequencies for LVCMOS18

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.001	0.014	0.133	1.326	13.262
Leakage	0.013	0.013	0.015	0.036	0.036
Total Power	0.015	0.029	0.172	1.599	15.527

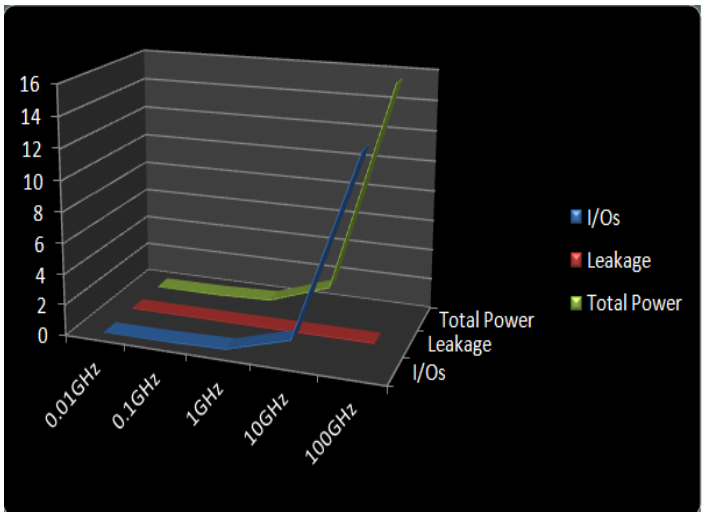

Figure5: Graph of I/Os, Leakage and Power at different frequencies for LVCMOS18

There is 90%, 98.99%, 99.89% and 100% reduction in IOs when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 0%, 58.33%, 63.88% and 63.88% reduction in Leakage when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 89.70%, 98.89%, 99.81% and 99.90% reduction in Total Power when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively.

Table 6: Values of I/Os, Leakage and Power for LVCMOS33

Frequency GHz	0.01	0.1	1	10	100
I/Os	0.003	0.034	0.331	3.309	33.090
Leakage	0.015	0.015	0.018	0.038	0.038
Total Power	0.018	0.052	0.374	3.583	35.356

There is 90%, 98.99%, 99.89% and 99.99% reduction in IOs when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 0%, 52.63%, 60.52% and 60.52% reduction in Leakage when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively. There is 89.86%, 98.94%, 99.85% and 99.94% reduction in Total Power when we scale down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, and 0.01GHz respectively.

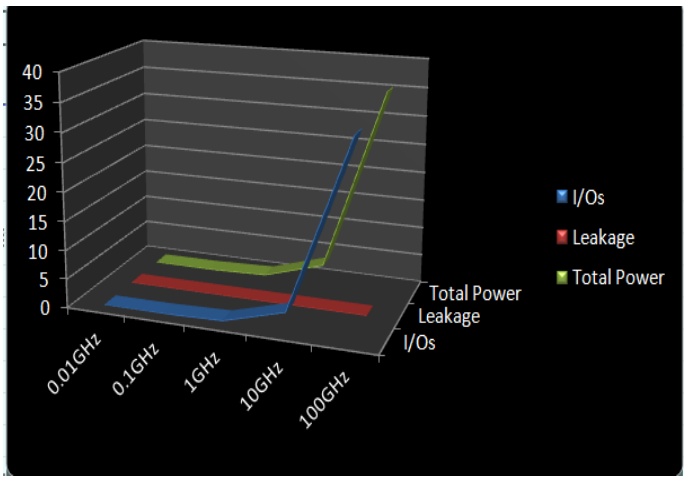

Figure 6: Graph of I/Os, Leakage and Power at different frequencies for LVCMOS33

4. CONCLUSION

Reductions in clock, logic, IOs, leakage and total power are noted down successfully and there graphs are also plotted for precise observations. It is very clear from tables that at higher value of frequencies more power is consumed and vice versa. This will help in designing low power digital clock for efficient output.Spartan-6 gives low power readings and so is efficient for designing of not only digital clock but various electronic designs. The frequency range used from 0.01GHz to 100GHz. For this frequency range the value of clock, logic and signal almost remains same but due to IOs and leakage there is noticeable difference in total power consumed. Work is done in order to have an efficient design.

5. FUTURE SCOPE

These results can be used in future for making efficient digital clocks. The work has been done on LVCMOS at various frequencies. Further various fields like output load or capacitance can be varied. Result can be noted for various families like Virtex-6,

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Virtex-5 and Virtex-4 etc. and form all outputs, best results are implemented for manufacturing process. Digital clocks are used in mobile phones and many electronics gadgets that's why it is important to make this useful device efficient and a lot of work can be done in this field further.

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