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FPGA Based Low Power Router Design Using High Speed Transeceiver Logic IO Standard

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***Abstract*— Communication is the major aspect that plays an important role in success of any organization. Information in the same way is another aspect as to have communication data or information is must. So with the help of computer networks it is possible to build an environment of communication and information. Router is main component of computer networks is an intelligent device uses to transfer data packets between various computer networks. Router must consume low power to perform its work in an efficient manner. To achieve the same the work has been done to make a FPGA based low power design using different standards of HSTL.**

Keywords- *Computer Networks, Router, HSTL, IO standards, FPGA, Power*

I. INTRODUCTION

This paper is based on designing a low energy FPGA based router design using different standards of HSTL. The software used for simulation is Xilinx. The different parameters are noted down at different frequencies and finally total reduction in total power consumed is noted down. Router is device that can connect different networks where as switch can be used in same network only. Router uses information from its routing table and gives direction to the packet. There are several types of routers which includes wired as well as wireless routers. The advantages of router are:

i. Routers can communicate between various networks which are having same or different domain.
ii. Routers afford us a secure network with the help of ACL and NAT.
iii. Routers can choose the finest path for data to its target.
iv. Router also limits the collision domain.

In this way router is very important component in computer networks and importantly needs to be energy efficient. This FPGA based router design using high speed transceiver logic is designed to full fill the energy requirements.

II. RELATED WORK

In order to attain low Power different parameters can be varied out like frequency, capacitance and leakage current etc. We have varied frequency for different families of

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high speed transceiver logic and conceive concerning the idea of lowering power consumption. Lot of work has been done with regard to

this aspect and some of relevant work is discussed in this particular section.

2.1 Simulation of High Speed Transceiver Logic Input Output standard based energy efficient frame buffer for digital image processor [1]

This paper aims to construct a buffer design which is achieved by using the various types of HSTL IO standards. The paper concentrates on same issue of low power consumption as much as possible. The paper compares the results of power consumption using Virtex6 FPGA and Airtex-7 FPGA. Uncommonly this paper the result is taken using Virtex6 and different parameters are evaluated at different values of frequency and then the total reduction in power is noted down.

2.2 Different Input Output Standard Based Energy Efficient Decoder Design For 64-bit Processor Architecture [2]

The paper emphasizes on designing a decoder that have 64-bit architecture by the analysis of I/O standards at various temperatures. The reduction of power in 28nm FPGA is calculated with LVCMOS but instead we have worked in reduction of power for an FPGA based router but using High Speed Transceiver Logic i.e. HSTL not low voltage complementary metal oxide. But the work in both the papers has been done in saving the energy of the systems and making them as efficient as possible.

2.3 Reduction of InputOut Power Using Energy Efficient HSTL I/O Standard in Vedic Multiplier on FPGA [3]

In this paper work is done to make Vedic multiplier energy efficient. The different standards of High speed Transceiver logic are used. The difference lies in the systems that we have done work to make router efficient where as in this paper multiplier is taken in to account. Both the designs are based on Field programmable gate array and I/O standards are taken in to consideration for calculating the total power consumed.

2.4 Simulation of High Speed Transceiver Logic Input Output standard based energy efficient Punjabi Unicode reader on FPGA [4]

This paper focuses on designing a Punjabi Unicode Reader that has Gurmukhi scripts on Field Programmable Gate Array. The design is observed at different frequencies of 25MHz, 125 MHz, 625 MHz, 1 GHz and 25 GHz. In router design the different values of power consumed are noted down at .01GHz, 0.1GHz, 1GHz, 10GHz and 100GHz.This Unicode reader has capability to count that how many number of vowel, number of consonants, and number of digits are present when it is used along with counter. Both the papers the HSTL standards for their designs based on FPGA.

2.5 Energy efficient vedic multiplier design using LVCMOS and HSTL IO standard [5]

In this vedic multiplier I/O standards of LVCMOS (Low Voltage Complementary Metal Oxide Semiconductor) and HSTL (High Speed Transceiver Logic are used in order to match the resistance of input and output line. Impedance matching is done to remove the transmission line reflection and thus to increase the stability of device. Percentage reduction in the leakage power and then in total power is calculated. Finally the objective lies in less dissipation of power and hence to make the system efficient.

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In addition to above discussed related work, Adder Design [6], Thermal Aware Object Tracking on FPGA [7] and Power Optimized Memory Circuit Using HSTL IO Standard on 28nm FPGA [8] have also worked on the same parameters using some similar standards and concepts for energy efficient design [9-12].

III. DATA ANALYSIS AND INTERPRETATION

A. Results

Table 1: Values of Clock, Logic and Signal at different Frequencies

Frequency GHz	0.01	0.1	1	10	100
Clocks	0.001	0.005	0.054	0.666	6.662
Logic	0.000	0.002	0.016	0.083	0.230
Signals	0.001	0.008	0.082	0.819	7.685

There is 90%, 99.1%, 99.9 % and 99.98% downgrading in the clock when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 63.9%, 93%, 99.1% and 100% downgrading in Logic when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 89.3%, 98.9%, 99.8% and 99.9% downgrading in Signals when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively.

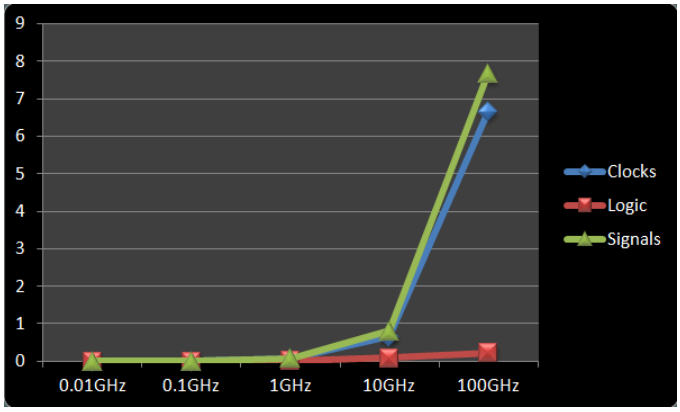

Fig 1: Graph of Clock, Logic and Signals at different frequencies

Table 2: Values of I/Os, Leakage and Power at different Frequencies for HSTL-I

Frequency GHz	0.01	0.1	1	10	100
I/Os	3.408	3.461	3.993	9.311	62.491
Leakage	0.768	0.770	0.783	0.929	1.028
Total Power	4.178	4.246	4.926	11.808	78.097

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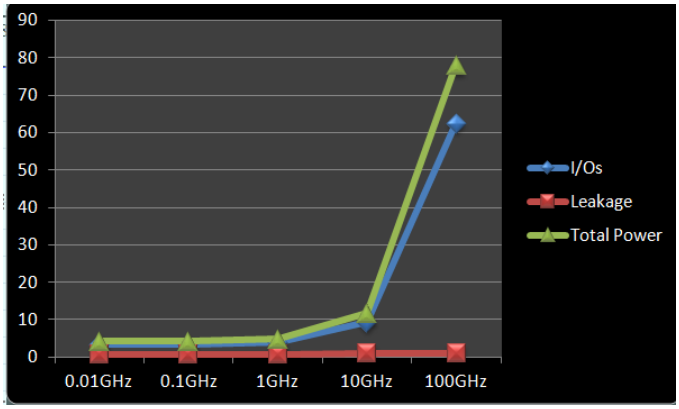

Fig 2: Graph of I/Os, Leakage and Power at different frequencies for HSTL-I

There is 85.1%, 93.6%, 94.4% and 94.5% downgrading in IOs when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 9.63%, 23.8%, 25.09% and 28.09% downgrading in Leakage when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 84.8%, 93.6%, 94.5.1% and 94.6% downgrading in Total Power when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively.

Table 3: Values of I/Os, Leakage and Power at different Frequencies for HSTL-II

Frequency GHz	0.01	0.1	1	10	100
I/Os	3.917	3.946	4.238	7.154	36.312
Leakage	0.778	0.779	0.788	0.879	1.028
Total Power	4.697	4.740	5.176	9.601	51.918

There is 80.2%, 88.32%, 89.13% and 89.21% downgrading in IOs when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 14.4%, 23.3%, 24.2% and 24.3% downgrading in Leakage when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 81.5%, 90.0%, 90.8% and 90.95% downgrading in Total Power when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively.

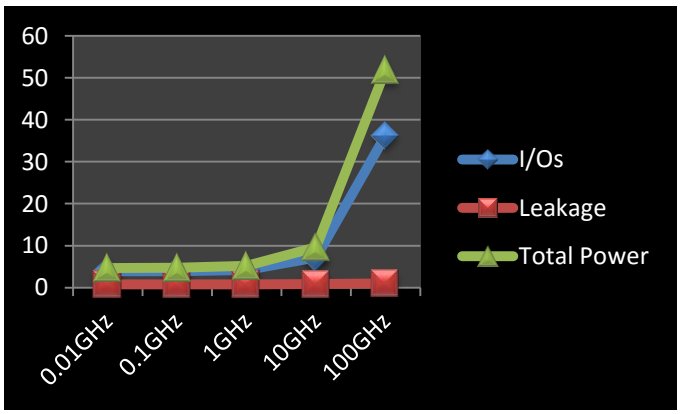

Fig 3: Graph of I/Os, Leakage and Power at different frequencies for HSTL-II

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Table 4:Values of I/Os, Leakage and Power at different Frequencies for HSTL-III

Frequency GHz	0.01	0.1	1	10	100
I/Os	3.14	3.097	3.924	12.197	94.920
Leakage	0.761	0.763	0.781	1.001	1.028
Total Power	3.777	3.875	4.856	14.766	110.525

There is 87.15%, 95.86%, 96.7% and 96.8% downgrading in IOs when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 2.6%, 24%, 25.7% and 25.9% downgrading in Leakage when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 86.6%, 95.6%, 96.4% and 96.5% downgrading in Total Power when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively.

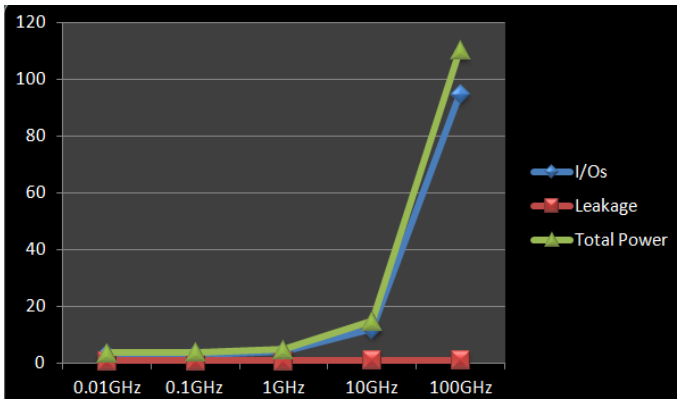

Fig 4: Graph of I/Os, Leakage and Power at different frequencies for HSTL-III

Table 5: Values of I/Os, Leakage and Power at different Frequencies for HSTL-III18

Frequency GHz	0.01	0.1	1	10	100
I/Os	3.051	3.150	4.144	14.078	113.425
Leakage	0.762	0.764	0.786	1.028	1.028
Total Power	3.814	3.929	5.080	16.675	129.031

There is 87.5%, 96.34%, 97.2% and 97.3% downgrading in IOs when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 0%, 23.5%, 25.6% and 29.3% downgrading in Leakage when we step down frequency from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively. There is 87.07%,

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96.06%, 96.9% and 97.04% downgrading in Total Power consumed when frequency is step down from 100GHz to 10GHz, 1GHz, 0.1GHz, 0.01GHz respectively.

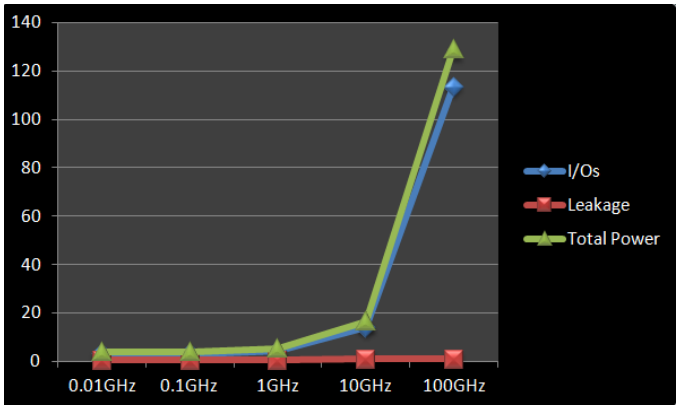

Fig 5: Graph of I/Os, Leakage and Power at different frequencies for HSTL-III18

IV. CONCLUSION

The work has been done to make an efficient router design. The values of different input output standards, leakage and total power consumed are taken at different values of frequencies. The whole data is properly examined and the total reductions in the different parameters are plotted graphically. This is done for different standards of High Speed transceiver logic i.e. HSTL-I, HSTL-II, HSTL-III and HSTL-III 18. Simulation is done using Xilinx ISE design suit 14.2 and we can conclude that there is a large reduction in total power consumed when the value of frequency is scaled down from 100GHz to 0.01GHz.

V. FUTURESCOPE

Since the need of computer networks is increasing day by day the need of efficient routers will definitely be there. So designing energy efficient router will increase the efficiency of the system and this can further be improved by using system on chip and virtex7.3-Dimensional Field programmable gate arrays can also be used in future. Further the results can be taken out at different frequencies and for different type of routers.

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