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Thermal Aware Energy Efficient RAM Design On FPGA

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Abstract—**In the project of low power processor design, we design both thermal aware and energy efficient RAM design on FPGA in this paper. This energy efficient and thermal aware RAM will be integrated in processor in order to make energy efficient and thermal aware processor. In order to test the compatibility of this design with the latest processor of i7 family, we operated this RAM with the highest frequencies supported by i7 processor. This RAM is thermal aware because it is able to operate without any fault or error with change in temperature from 50ºC to 80ºC. This RAM is energy efficient because it is able to operate with less power without any compromise with performance and functionality of RAM. There are 74.54% reduction in clock power, 75.36% reduction in I/O power, 0.42% reduction in leakage power and 11.74% reduction in leakage power in special case of no peak demand of high performance (4GHz).**

Keywords—Junction Temperature, Ambient Temperature, Leakage Power, Clock Power, I/O Power, RAM, Energy Efficient

I. INTRODUCTION

RAM, random access memory, are classified into SRAM and DRAM. DRAM is using one transistor and one capacitor. Whereas, SRAM is made with six transistors. Due to involvement of capacitor, DRAM require charge refreshment operation after each read or after each periodic interval. SRAM is used in cache and DRAM is used in primary memory. Our design RAM [1-2,7] is both thermal aware [4-5] and energy efficient [3,6]. Thermal aware RAM means it is operating without any fault or error with change in temperature from 50ºC to 80ºC. Energy efficient RAM is design which is able to operate with less power than the traditional RAM. If there is scope to reduce power dissipation without any compromise with performance, then we classify that VLSI design into energy efficient design.

Table 1: Specification of 4^{th} Generation i7 Processor

i7 Processor	Frequency (GHz)	#f Cores
4610Y	2.9	4
4600U	3.3	2
4600M	3.6	2
4960HQ	3.8	2
4790K	4.0	4

In order to test the compatibility of our design RAM with the latest processor in i7 family, we are operating our RAM with device operating frequency of 2.9GHz,

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3.3GHz, 3.6GHz, 3.8GHz and 4.0GHz. During thermal analysis of our design RAM, we are operating our RAM with these 5 different operating frequencies under the influence of proper heat sink profiling and airflow. The unit of airflow is LFM. LFM is linear feet per minute. Medium profile and high profile heat sink are two different heat sinks taken under consideration. Similarly, 500 and 250 LFM are taken under consideration in our experiment.

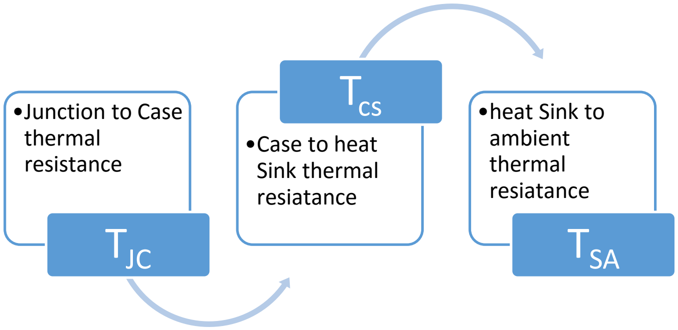

Figure 1: Junction to Ambient Thermal Resistance (T_{JA})

TJA decides the increase in temperature with per unit power dissipation. Unit of TJA is ^{o}C/W. For example, if TJA is 2.9 that means there will increase of 2.9^{o}C in junction temperature with unit power dissipation i.e. 1W. Power is measured in Watt (W). Clock power and I/O power are constituents of dynamic power. Leakage power is also called static power. Total power is a sum total of dynamic power and Total power. Dynamic power is directly proportional to frequency and static power is directly proportional to temperature. In this work, our design parameters are frequency and temperature, which is needed to make thermal aware and energy efficient RAM design.

II. Power Analysis

A. *Using 250 LFM Airflow and Medium Profile Heat Sink*

Table 2: Power Dissipation at 50^{o}C Ambient Temperature

Power→ Frequency↓	Clock	I/O	Leakage	Total Power
1GHz	0.014	0.017	0.712	0.744
2.9GHz	0.040	0.050	0.714	0.807
3.3GHz	0.045	0.057	0.714	0.820
3.6GHz	0.049	0.062	0.714	0.830
3.8GHz	0.052	0.065	0.714	0.836
4.0GHz	0.055	0.069	0.715	0.843

There are 74.54% reduction in clock power, 75.36% reduction in I/O power, 0.42% reduction in leakage power and 11.74% reduction in leakage power in special case of no peak demand of high performance (4GHz) as shown in Table 2.

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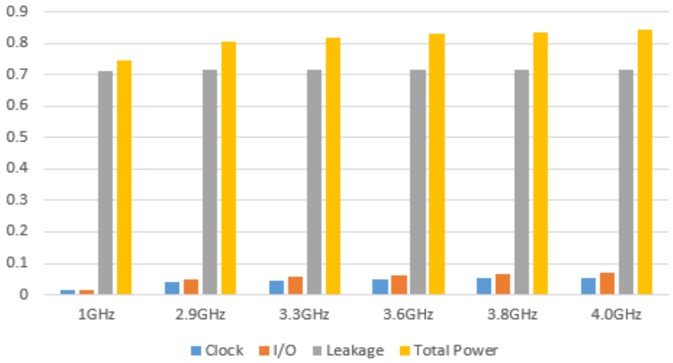


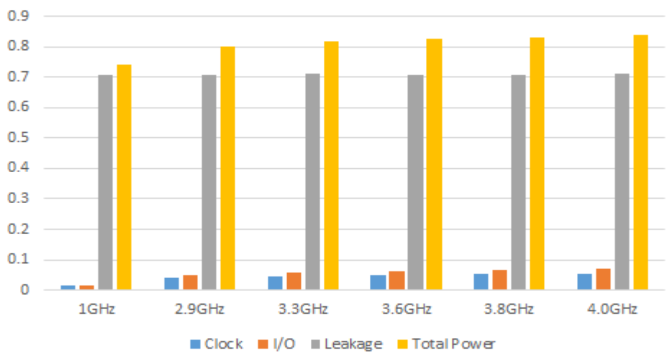
Figure 2: Power Dissipation for Different Frequency

B. Using 500 LFM Airflow and High Profile Heat Sink

Table 3: Power Dissipation at 50^{o}C Ambient Temperature

Power→ Frequency↓	Clock	I/O	Leakage	Total Power
1GHz	0.014	0.017	0.708	0.740
2.9GHz	0.040	0.050	0.709	0.802
3.3GHz	0.045	0.057	0.712	0.818
3.6GHz	0.049	0.062	0.709	0.825
3.8GHz	0.052	0.065	0.709	0.831
4.0GHz	0.055	0.069	0.710	0.838

When we upgrade heat sink profile and change airflow to 500 LFM, then there are no change in clock power and I/O power. In similar case, there are significant change in leakage power and total power in compare to power dissipation with 250 LFM and medium profile heat sink as shown in Table 3 and Figure 3.



C. Using 250 LFM Airflow and Medium Profile Heat Sink

Table 4: Power Dissipation at 60^{o}C Ambient Temperature

Power→ Frequency↓	Clock	I/O	Leakage	Total Power
1GHz	0.014	0.017	0.798	0.830
2.9GHz	0.040	0.050	0.799	0.892
3.3GHz	0.045	0.057	0.800	0.906
3.6GHz	0.049	0.062	0.800	0.916
3.8GHz	0.052	0.065	0.800	0.922
4.0GHz	0.055	0.069	0.800	0.929

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When we change ambient temperature from 50°C to 60°C, then there is no change in clock power and I/O power as shown in Figure 3-4.

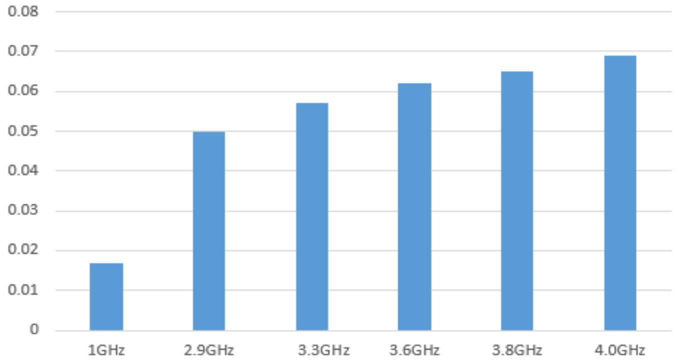

Figure 3: IO Power Dissipation on 50 °C, 60 °C, 70 °C, 80 °C

D. Using 500 LFM Airflow and High Profile Heat Sink

Table 5: Power Dissipation at 60°C Ambient Temperature

Power→ Frequency↓	Clock	I/O	Leakage	Total Power
1GHz	0.014	0.017	0.792	0.824
2.9GHz	0.040	0.050	0.793	0.836
3.3GHz	0.045	0.057	0.794	0.899
3.6GHz	0.049	0.062	0.794	0.901
3.8GHz	0.052	0.065	0.794	0.916
4.0GHz	0.055	0.069	0.794	0.922

High profile heat sink and airflow don't create any effect on clock power and I/O power. High profile heat sink and airflow are responsible for significant change in leakage power and total power in compare to power dissipation with 250 LFM and medium profile heat sink as shown in Table 5.

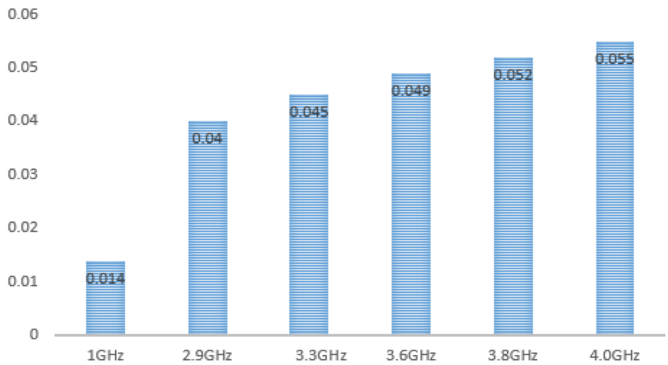

Figure 4: Clock Power Dissipation on 50°C, 60°C, 70°C, 80°C

E. Using 250 LFM Airflow and Medium Profile Heat Sink

Table 6: Power Dissipation at 70°C Ambient Temperature

Power→ Frequency↓	Clock	I/O	Leakage	Total Power
1GHz	0.014	0.017	0.896	0.928
2.9GHz	0.040	0.050	0.898	0.991
3.3GHz	0.045	0.057	0.898	1.004

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3.6GHz	0.049	0.062	0.898	1.014
3.8GHz	0.052	0.065	0.898	1.020
4.0GHz	0.055	0.069	0.899	1.027

With further change in ambient temperature from 50^{o}C to 70^{o}C, there are 74.54% reduction in clock power, 75.36% reduction in I/O power, 0.34% reduction in leakage power and 9.64% reduction in total power when we scale down device operating frequency from 4GHz to 1GHz as shown in Table 6.

F. *Using 500 LFM Airflow and High Profile Heat Sink*

Table 7: Power Dissipation at 70^{o}C Ambient Temperature

Power→ Frequency↓	Clock	I/O	Leakage	Total Power
1GHz	0.014	0.017	0.889	0.921
2.9GHz	0.040	0.050	0.890	0.983
3.3GHz	0.045	0.057	0.890	0.996
3.6GHz	0.049	0.062	0.890	1.006
3.8GHz	0.052	0.065	0.891	1.012
4.0GHz	0.055	0.069	0.891	1.019

With 70^{o}C ambient temperature along with 500 LFM and high profile heat sink, there are 74.54% reduction in clock power, 75.36% reduction in I/O power, 0.34% reduction in leakage power and 9.64% reduction in total power when we scale down device operating frequency from 4GHz to 1GHz as shown in Table 7.

G. *Using 250 LFM Airflow and Medium Profile Heat Sink*

Table 8: Power Dissipation at 80^{o}C Ambient Temperature

Power→ Frequency↓	Clock	I/O	Leakage	Total Power
1GHz	0.014	0.017	1.008	1.040
2.9GHz	0.040	0.050	1.010	1.103
3.3GHz	0.045	0.057	1.011	1.116
3.6GHz	0.049	0.062	1.011	1.126
3.8GHz	0.052	0.065	1.011	1.133
4.0GHz	0.055	0.069	1.011	1.140

With 80^{o}C ambient temperature along with 250 LFM and medium profile heat sink, there are 27.27% reduction in clock power, 27.54% reduction in I/O power, 0.01% reduction in leakage power and 3.25% reduction in total power when we scale down device operating frequency from 4GHz to 2.9GHz as shown in Table 8.

H. *Using 500 LFM Airflow and High Profile Heat Sink*

Table 9: Power Dissipation at 80^{o}C Ambient Temperature

Power→ Frequency↓	Clock	I/O	Leakage	Total Power
1GHz	0.014	0.017	0.999	1.031
2.9GHz	0.040	0.050	1.000	1.093
3.3GHz	0.045	0.057	1.001	1.106
3.6GHz	0.049	0.062	1.001	1.116

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3.8GHz	0.052	0.065	1.001	1.123
4.0GHz	0.055	0.069	1.001	1.130

With 80^{o}C ambient temperature along with 500 LFM and high profile heat sink, there are 18.18% reduction in clock power, 17.39% reduction in I/O power, 0% reduction in leakage power and 2.13% reduction in total power when we scale down operating frequency from 4 to 3.3GHz as shown in Table 9.

III. THERMAL ANALYSIS

A. *When Device Operating Frequency is1.0 GHz*

Table 10: Leakage Power Analysis of Energy Efficient RAM on 1.0 GHz

Power→ Frequency↓	Leakage with 250 LFM	Leakage with 500 LFM
50^{o}C	0.712	0.708
60^{o}C	0.798	0.792
70^{o}C	0.896	0.889
80^{o}C	1.008	0.999

There are 0.56%, 0.75%, 0.78%, and 0.89% reduction in leakage power with 500 LFM at 50 ^{o}C, 60 ^{o}C, 70 ^{o}C, and 80 ^{o}C respectively as shown in Table 10 and Figure 5. When we scale down ambient temperature from 80oC to 50oC, there is 29.36% reduction in leakage power.

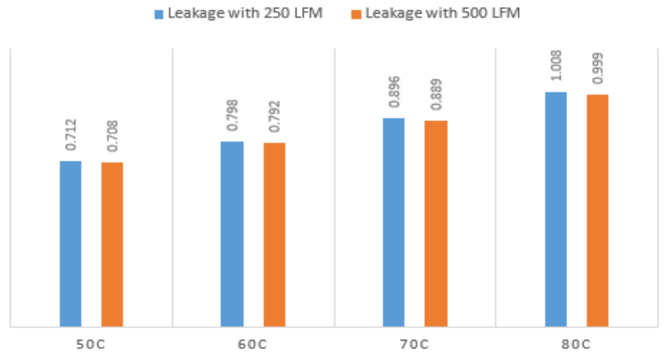

Figure 5: Leakage Power with Different Airflow

B. *When Device Operating Frequency is2.9 GHz*

Table 11: Leakage Power Analysis of Energy Efficient RAM on 2.9 GHz

Power→ Frequency↓	Leakage with 250 LFM	Leakage with 500 LFM
50^{o}C	0.714	0.709
60^{o}C	0.799	0.793
70^{o}C	0.898	0.890
80^{o}C	1.010	1.000

There are 0.7%, 0.75%, 0.89%, and 0.99% reduction in leakage power with 500 LFM at 50 ^{o}C, 60 ^{o}C, 70 ^{o}C, and 80 ^{o}C respectively as shown in Table 11 and Figure 6. When we scale down ambient temperature from 80oC to 50oC, there is 29.31% reduction in leakage power.

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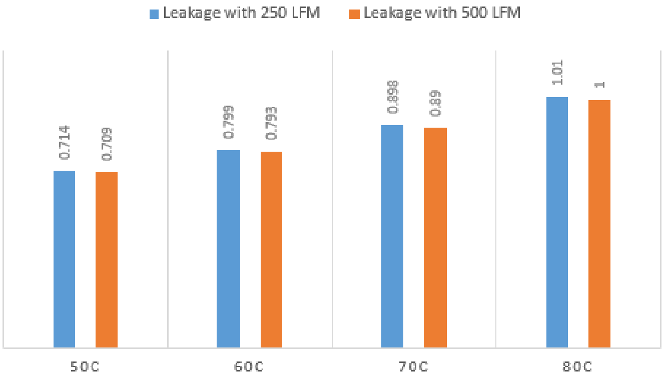

Figure 6: Leakage Power with Different Airflow

C. *When Device Operating Frequency is3.3 GHz*

Table 12: Leakage Power Analysis of Energy Efficient ROM on 3.3 GHz

Power→ Frequency↓	Leakage with 250 LFM	Leakage with 500 LFM
50°C	0.714	0.712
60°C	0.800	0.794
70°C	0.898	0.890
80°C	1.011	1.001

There are 0.28%, 0.75%, 0.22%, and 0.98% reduction in leakage power with 500 LFM at 50 °C, 60 °C, 70 °C, and 80 °C respectively as shown in Table 12 and Figure 6. When we scale down ambient temperature from 80°C to 50°C, there is 29.38% reduction in leakage power.

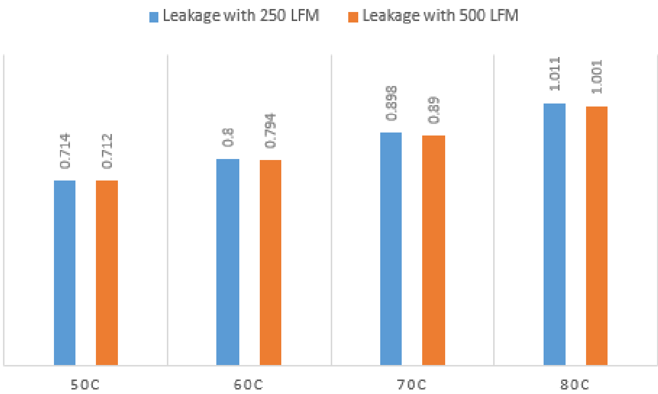

Figure 7: Leakage Power with Different Airflow

D. *When Device Operating Frequency is3.6 GHz*

Table 13: Leakage Power Analysis of Energy Efficient ROM on 3.6 GHz

Power→ Frequency↓	Leakage with 250 LFM	Leakage with 500 LFM
50°C	0.714	0.709
60°C	0.800	0.794
70°C	0.898	0.890
80°C	1.011	1.001

There are 0.70%, 0.75%, 0.89%, and 0.98% reduction in leakage power with 500 LFM at 50 °C, 60 °C, 70 °C, and 80 °C respectively as shown in Table 13 and Figure 8. When

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we scale down ambient temperature from 80°C to 50°C, there is 29.38% reduction in leakage power.

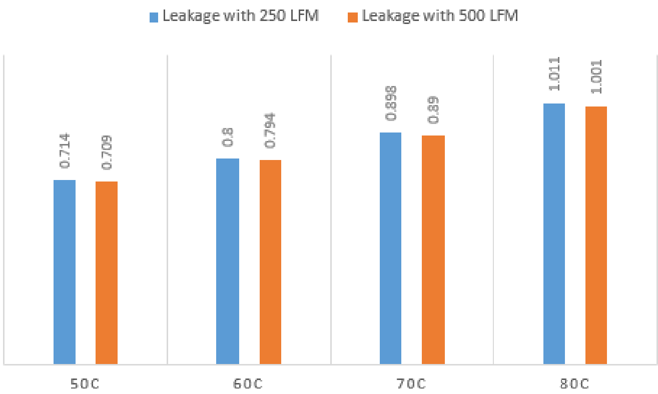

Figure 8: Leakage Power with Different Airflow

E. When Device Operating Frequency is4.0 GHz

Table 14: Leakage Power Analysis of Energy Efficient ROM on 4.0 GHz

Power→ Frequency↓	Leakage with 250 LFM	Leakage with 500 LFM
50°C	0.715	0.710
60°C	0.800	0.794
70°C	0.899	0.891
80°C	1.011	1.001

There are 0.69%, 0.75%, 0.89%, and 0.98% reduction in leakage power with 500 LFM at 50 °C, 60 °C, 70 °C, and 80 °C respectively as shown in Table 14 and Figure 9. When we scale down ambient temperature from 80°C to 60°C, there is 20.87% reduction in leakage power.

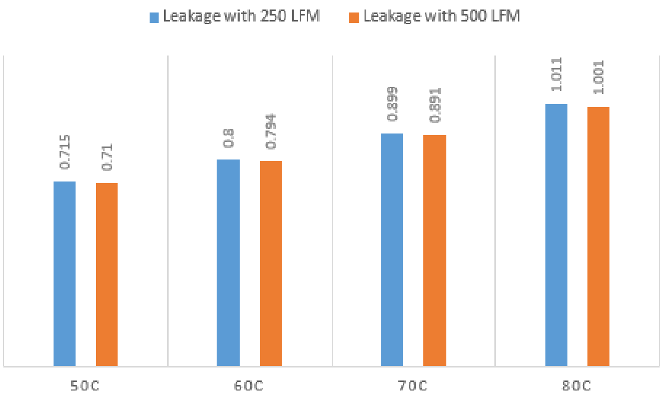

Figure 9: Leakage Power with Different Airflow

IV. Conclusion

This work is a part of the low power and thermal aware processor design project. Our design is both thermal aware and energy efficient RAM design on FPGA. This design has passed the compatibility test with the latest processor of i7 family. This RAM is thermal aware because it is able to operate without any fault or error with change in temperature from 50°C to 80°C. This RAM is energy efficient because it is able to

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operate with less power and deliver same output. There are 74.54% reduction in clock power, 75.36% reduction in I/O power, 0.42% reduction in leakage power and 11.74% reduction in leakage power at 1GHz in compare to the special case of no peak demand of high performance (4GHz).

V. FUTURE SCOPE

In this work, we are designing RAM in Verilog and implement on Virtex-5 FPGA. There is wide scope to design this RAM on 40nm FPGA, 28nm FPGA and ultra-scale FPGA. We can also use thermal aware design approach in other thermal aware circuits like ROM, ALU, and FIR filter and so on.

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